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Fabrication and Characterization of Novel 2SSS CIGS Thin Film Solar Cells for Large-Scale Manufacturing

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Fabrication and Characterization of Novel 2SSS CIGS Thin Film Solar Cells for Large-

Scale Manufacturing

by

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A thesis submitted in partial fulfillment
of the requirements for the degree of
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DEDICATION

This thesis is dedicated to my parents S.Gnana Mohan and K.Sarala, who took care with

all their love, supported and believed in me. To my professor Dr. Don Morel, who

guided, instructed and inspired me in the graduate school.

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ABSTRACT

A novel 2SSS (2 Step Solid Selenization) CIGS (Cu, In, Ga, Se) thin film solar cell recipe was developed which can be a replacement to the conventional co-deposition process usually employed for large-scale manufacturing. The co-deposition procedure is faced with multiple problems such as selenium incorporation, effective gallium incorporation in the absorber. It is a 2-step proprietary procedure with better control over growth mechanisms and material utilization for the absorber layer for the CIGS thin film solar cells. It makes use of solid selenium source as preferred by manufacturers. Each step of the 2-step procedure was dealt with separately for stoichiometric analysis and interesting trade-offs between materials such as gallium, indium and selenium was found. Solar cells with this proprietary absorber were fabricated on soda lime glass substrates. Results of the solar cells made with the 2SSS process matched with that of the co-deposition process with the quantum efficiencies near 80% of the co-deposition cells. These experiments are going to serve as the test bed for the pilot line that is intended to be installed at USF's research campus soon. The finished solar cells were characterized. The scanning electron microscope (SEM), energy dispersive spectroscopy (EDS) and X-ray diffraction (XRD) were some of the important tools during the analysis of stoichiometry and structural properties. The device performances were measured with the help of current-voltage (I-V) testing and quantum efficiency (QE) measurements.

CHAPTER 1   SEMICONDUCTOR PHYSICS

1.1   Introduction

Ever wondered about a source of energy that would last for 5 billion years from present? There is a source that would last this long; I doubt whether even life would exist then. But I am talking about solar energy. Sun is "cool" enough to let life exist on earth and also provide humans with energy to lead a pleasant life. All we human beings need to do is to extract this energy in the right way. Do you think it's easy?? We can give it a try, which is what drove me to research on Solar cells. We boast of different industries being set up in the developed and developing countries each day, but do we ever think how are these industries going to be powered? I feel only renewable energy sources are the future. To be frank I get scared when some people say if there is world war next it would be for energy acquirement. Energy requirements are serious issues and are of immediate concerns for any nation today.

I feel solar power stands out from other renewable energy sources of because of its availability and accessibility. Large scale manufacturing is facing many challenges. Solar cells are used to convert energy from sun to electricity. This study deals with a specific type of solar cells called CIGS thin film solar cells.

1.2   Photovoltaics

The science of converting solar energy to electrical energy is called photovoltaics. This effect was first reported by Edmund Bequerel in 1839 when he observed that the action of light on a silver coated platinum electrode immersed in electrolyte produced an electric current [1]. It was Charles Fritts who prepared the first large area solar cell by pressing a layer selenium between gold and another metal [1]. Later photovoltaic effects were found in compounds such as copper-oxide thin film structures, in lead sulphide and thallium sulphide [1]. As described above the initial solar cells were of thin film Schottky barrier where there was an asymmetric junction between metal layer and semiconductor. With the evolution of silicon electronics all these changed as there was the introduction of p-n junction. The p-n junctions provided much better rectifying actions compared to that of Schottky barriers and hence a better photovoltaic behavior. This led to the development of a silicon solar cell of 6% efficiency by Chapin, Fuller & Pearson in 1954. Later different p-n junction devices of gallium arsenide, indium phosphide and cadmium telluride were studied. The cost of such solar cells was a whopping $200 per watt. It was later in the 1990s, when the nations started experiencing oil shortages and were in search of different sources of energy that led to photovoltaic production expansion. Soon there was a noticeable 15-20% growth per annum in photovoltaic production which led to the cost reduction. Ways to lower costs were also eased by the finding of new amorphous, polycrystalline, thin film and organic conductors. Top CIGS thin film companies like Global solar, Nano-Solar now claim a cost of $1 or less per watt due to extensive development in the deposition techniques.

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1.3 Physics Involved in Semiconductors and Solar Cells

1.3.1 Semiconductors

Semiconductors are materials whose conductivity lies between that of a metal and an insulator. They form a special category of materials in large part because of their electrical, optical and material characteristics. The band diagram of a semiconductor is as shown in the below Figure 1. The energy gap E_g between the valence band and the conduction band is not as big as in insulators or overlapping as in case of conductors.
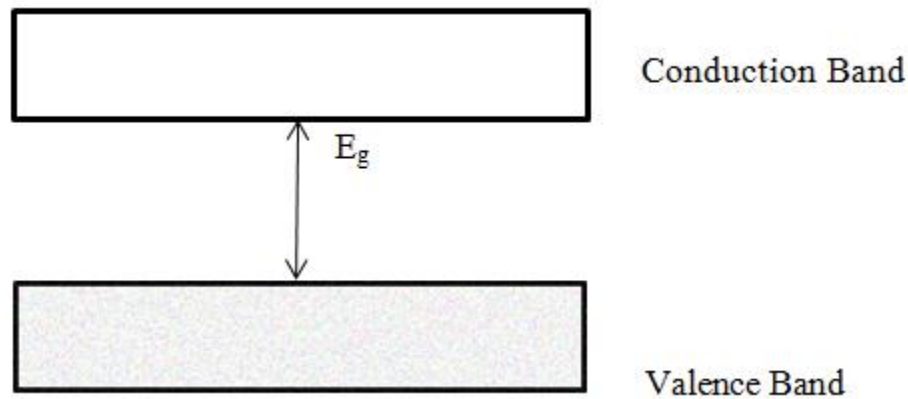
Figure 1 Energy band diagram of a semiconductor

1.3.2 Doping

Semiconductor in its purest form is called intrinsic. When a semiconductor is incorporated with certain impurities its crystal structure gets disturbed and exhibits interesting features. This process is called doping. The introduced impurities will have bonds of different strengths compared to that of a perfect crystal and hence will change the local distribution of the electron energy levels. Basically there are two types of impurities: donor impurity & acceptor impurity. When a semiconductor gets doped to

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have an increased density of electrons compared to holes in them, it is called n-type doping and the impurity is called donor type, as it donates extra electrons. While an impurity which increases the density of positive charges compared to negative charges in a semiconductor is called acceptor impurity and the corresponding doping type is p-type.

1.4 P-N Junction

On doping a semiconductor with p-type and n-type there is an interface between them. This results in what is called the p-n junction. The junction is depicted in the Figure 2. This region is depleted of both electrons and holes. There is a tendency of the holes from the p-type region to move towards the n-type region leaving behind ionized acceptor. Likewise the electrons from the n-type material move towards the p-type leaving behind ionized donors. The region comprising the ions form what is known as the space charge region as depicted in the Figure 2. Presence of charges on the two extremes gives rise to a built in potential as in Equation 1.

$$V_{bi} = kT/q * \ln(N_A N_D / n_i{}^2)$$

Equation 1 Built in potential [1]

The width of the space charge region is also decided by similar parameters and hence is given by

$$W = [2\varepsilon(V_{bi} - V) * ((N_A + N_D))]^{1/2} / q * (N_A N_D)^{1/2}$$

Equation 2 Width of space charge region [1]

where,

N_A is Acceptor impurity concentration on the p-side of the junction

N_D is Donor impurity concentration on the n-side of the junction

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V is Applied voltage

k is Boltzmann's constant

T is Temperature

n_i is Intrinsic carrier concentration
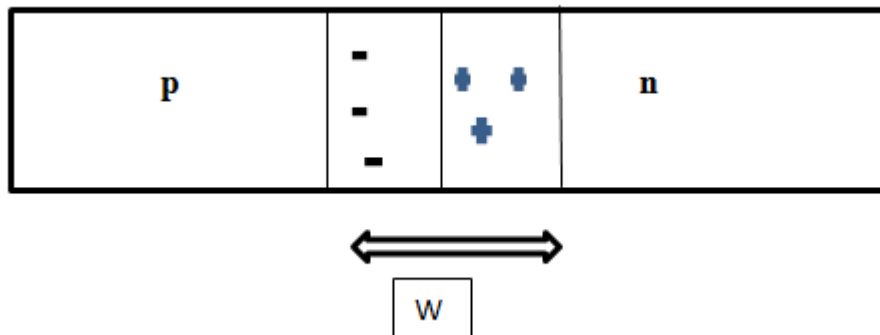
Figure 2 Schematic of a p-n junction

1.4.1 Biased P-N Junction

The p-n junction can be biased by connecting it to an external power supply. If the p-n junction is connected in such way that the p-region is connected to positive terminal of the supply and n-region is connected to the negative terminal then it is forward biased. In such a case the electrons in the n-region and the holes from the region gain sufficient energy to crossover the lowered potential energy barrier. This results in the current flow across the junction. The current in the forward biased condition is due to the majority charge carriers and is called diffusion current .The current v/s voltage characteristics under forward biased condition is as shown in Figure 3. When the p-n junction's p-region is connected to the negative terminal of the external power supply and the n-region is connected to the positive terminal it is said to be reverse biased. In such a case the

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majority carriers are attracted towards the power supply terminals and hence diffusion current becomes negligible. However due to the presence of electron-hole pairs generated due to thermal energy there will be small leakage current under reverse bias. The current flowing across the junction can be represented by the Equation 3.

$$I = I_{SAT} \exp((qV/kT) - 1)$$

Equation 3 P-N junction current [1]

where,

I_{SAT} = Saturation current
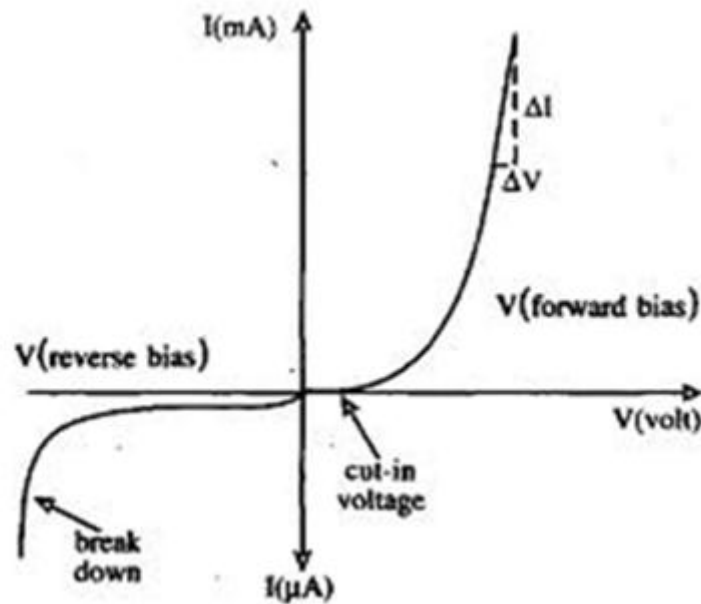
Figure 3 I-V characteristics of a p-n junction [21]

1.5 Heterojunction

A junction formed by semiconductors with dissimilar energy band gaps is called heterojunction. Such devices are of extreme importance in optoelectronics. It is very important for a solar cell to consist of semiconductors of different energy band gaps so as

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to match various parts of the solar spectrum. Let us consider a condition where a typical solar cell which consists of n-on-p heterojunction with the energy levels E_{g1} and E_{g2} respectively with $E_{g1}>E_{g2}$. Now the light with energy less than E_{g1} but greater than E_{g2} will be absorbed by the semiconductor layer at the bottom. So the n-type top layer acts as a window layer. Taking a look at the energy band diagram during the formation of heterojunction in Figure 4 we can notice there are discontinuities formed.
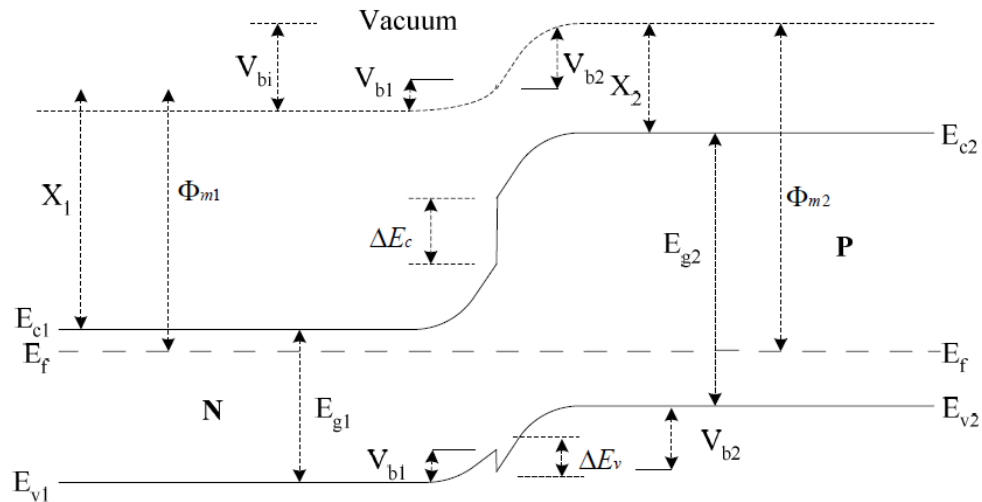
Figure 4 Band diagram after the heterojunction formation [3]

The formed discontinuities in the valence and conduction band serves as an initiation for the carrier flow in the solar cells under light. Difference in properties such as electron affinities can be the reason for such discontinuities. The discontinuities are given by

$$\Delta E_C = X_1 - X_2$$

Equation 4 Discontinuity in conduction band

$$\Delta E_V = (E_{g2} - E_{g1} - \Delta E_C)$$

Equation 5 Discontinuity in the valence band

V_{bi} is the total built in potential which is a sum of electrostatic potentials V_{b1} and V_{b2} of the two semiconductors, while X_1 and X_2 are the respective affinities of the semiconductors.

1.6 Solar Cells

Solar cells are devices made of various n and p type semiconductors that convert light energy to electrical energy. Each of the semiconductors has different band gaps which enables it to match with different regions on the solar spectrum. When light is incident on a solar cell the light of energy less than that of the energy band gap of the semiconductor the corresponding layer absorbs it. Light consists of packets of photons, when these photons are absorbed they in turn generate what is called as EHP (Electron-Hole Pair). The generated carriers can be driven across the junction to an external circuit or load in the presence of an electric field to be collected at the contacts at the extreme ends of the device. Such a current is called the photocurrent. Hence it becomes very clear that selecting what semiconducting material makes the solar cell is a critical issue. This is because each material has different absorption coefficient. The Equation 6 gives the relation between incident intensity and absorption coefficient of a semiconductor.

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$$I = I_O[\exp(-\alpha(\lambda)t)]$$

Equation 6 Photocurrent [2]

where,

I_O = Intensity of light incident on the semiconductor

α = Absorption coefficient

λ = Wavelength of incident light

t = Depth of material the light travels into from the surface of incidence

1.6.1   Spectral Response

It is very important to determine how a solar cell responds to different parts of the solar spectrum. Typically for a thin film CIGS solar cell we do a spectral response that ranges from wavelengths 400nm-1400nm of light in order to determine its quantum efficiency. Quantum efficiency QE (E) refers to the ability of an incident photon of energy E on the solar cell to deliver an electron to the external circuit. I would like to quote a very important equation of the rate of carriers generated which is given by

$$G(\lambda, X) = \alpha(\lambda)F(\lambda)[1 - R(\lambda)]e^{-\alpha(\lambda)x}$$

Equation 7 Rate of photo generated carriers [2]

where,

x = distance from the semiconductor surface where EHPs' are generated

F (λ) = No. of incident photons /cm^2/s/unit bandwidth

R (λ) = Fraction of these photons reflected from surface

1.6.2 Equivalent Circuit of a Solar Cell
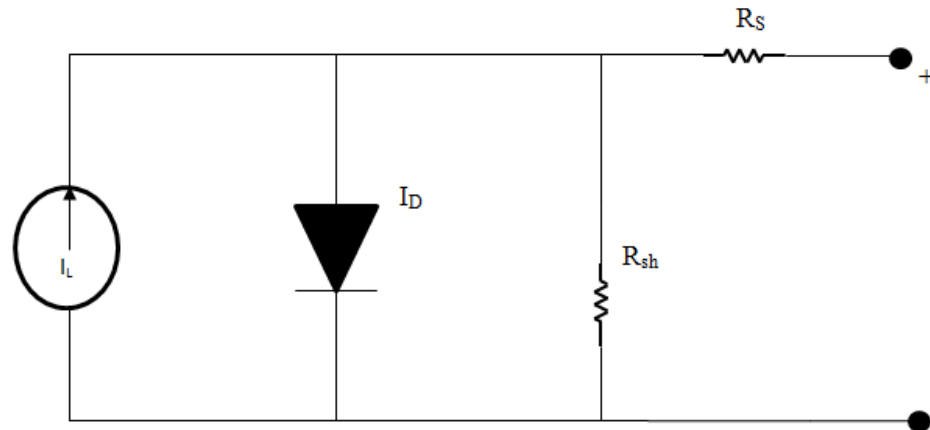
Figure 5 Equivalent circuit of a solar cell [1]

The equivalent circuit has a current source indicating I_L which is the photocurrent. Basically the solar cell is a current generator in parallel with a non-linear resistive device like a diode [1]. This is because when the solar cell is being illuminated it generates a photocurrent which varies w.r.t the variable resistance of the diode and light intensity. The resistance R_{sh} arises due to leakage current through the cell at the edges of the devices and contacts of different polarity. The series R_s is a result of resistance of the cell material to the flow of current and also the resistive contacts [1].

1.6.3 Important Parameters of a Solar Cell

Solar cell under illumination gives rise to photocurrent. In order to write an equation for the total current in a solar cell we take into account the voltage driven current and the light generated current. Hence the Equation 8 becomes

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$$I = I_{sat} \exp((qV/nkT) - 1) - I_L$$

Equation 8 Photocurrent under illumination [1]

where,

n = diode ideality factor

Under illumination the solar cell is said to be shorted and hence the short circuit current known I_{SC} is same as I_L. The ratio of I_{SC} over a particular cell area gives us the current density J_{SC}. The voltage obtained by setting I=0 in Equation 8 gives us what is known as the open circuit voltage V_{OC} of a solar cell.

$$V_{OC} = (kT/q) * \ln[(I_L/I_{SAT}) + 1]$$

Equation 9 Open circuit voltage [1]

Now when at certain point of I-V when the power becomes maximum we define a very important parameter of a solar cell called as the fill factor (FF).

$$FF = (V_M I_M)/(V_{OC} J_{SC})$$

Equation 10 Fill-factor [1]

Hence now the efficiency of the solar cell will be given by,

$$\eta = FF * V_{OC} * I_{SC}/(P_i)$$

Equation 11 Efficiency [1]

where,

P_i = input power

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1.6.4 I-V Characteristics

Current-voltage relationships of a solar cell in the dark and in the light are of importance. When there is no illumination the solar cell is said to be in dark. Even in this case there exists a very negligible current in the cell due to the minority charge carriers. However it is different under light as it is due to EHPs' and called the photo-generated current. To give you an idea I show you the I-V curves of one of 2SSS CIGS co-deposition cell sample SC32 that was made during the course of my research in Figure 6 and Figure 7. It is to be noted in the I-V curves the current densities (J) are calculated by multiplying a factor of 10 to the currents (I) as the areas of our devices are 0.1 cm^2.
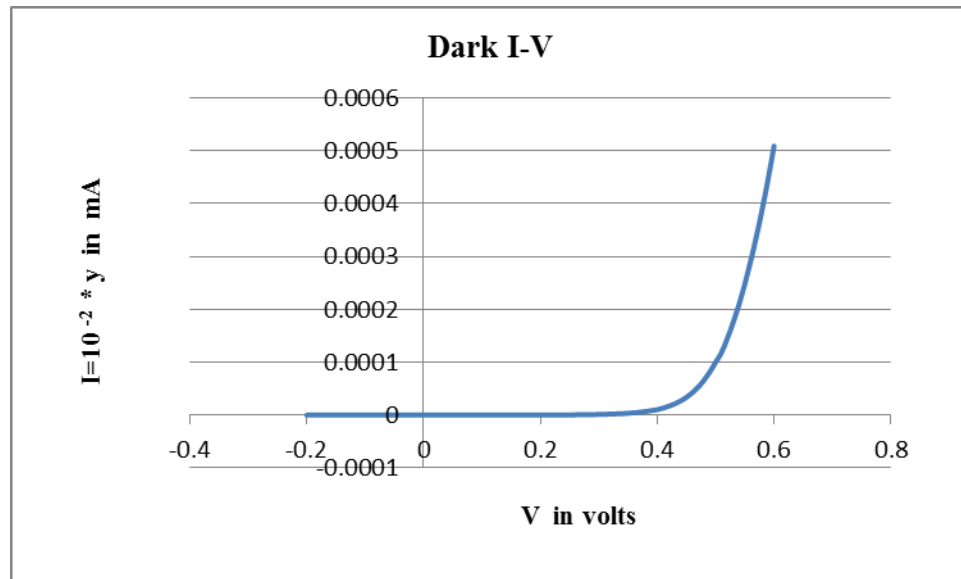
Figure 6 Current-voltage relation when solar cell is in the dark

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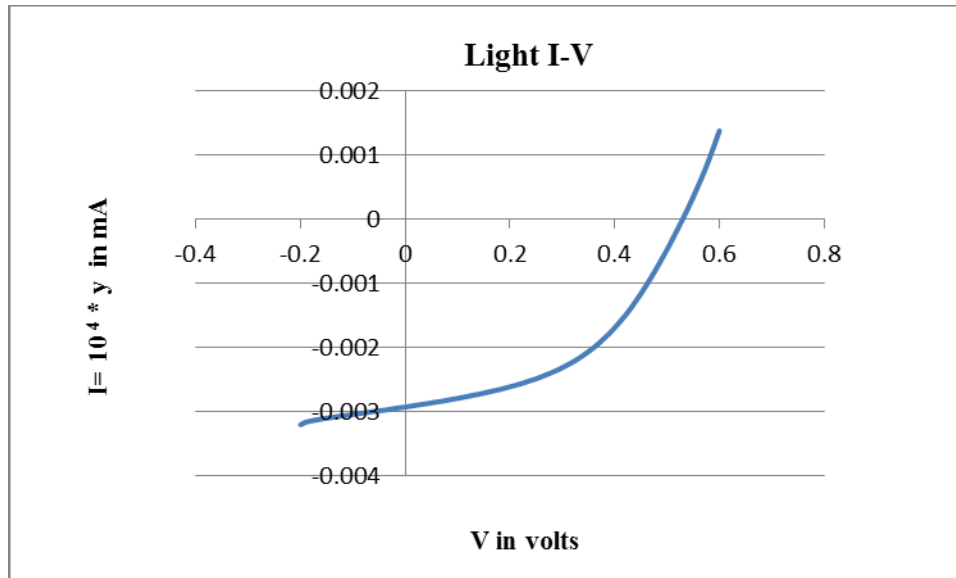
Figure 7 Current-voltage relation when solar cell is in the light

CHAPTER 2   CIGS THIN FILMS AND RESEARCH BACKGROUND

In this chapter an overview of various technologies used in the Photovoltaic (PV) industry will be presented. Focus will be on CIGS thin film solar industry. Different efforts taken to commercialize and new trends in the CIGS industry also will be covered. As explained earlier our aim through the thesis work is to establish a method for the commercialization of the CIGS thin film solar cells.

2.1   Why Thin Films?

The word thin itself indicates less material goes into the making. Material utilization is one of the major problems the PV industry is facing when it comes to commercialization of ideas. Thin film solar cells are what many have resorted in order to tackle this issue. This makes it feasible for large-scale production. The deposition techniques involved allow the making of certain novel compound semiconductors which otherwise wouldn't be possible [2]. The deposition techniques are flexible enough for the deposition to be on substrates such as glass, flexible substrates, polymer substrates etc. Certain electrical and optical properties that would not have existed in case of a same single crystal structure deposition becomes available [2]. A few of the very important deposition techniques for thin film includes thermal evaporation, sputtering, CVD (Chemical Vapor Deposition), ALD (Atomic Layer Deposition) etc. I would be discussing a few of these techniques in my next chapter as I tell about fabrication of my

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solar cells. However the major disadvantage of a thin film solar cell being the high density of defects in their lattices compared to a single crystal structure [2].

The major requirement of thin film solar cells are that thickness of the active semiconductor film must be greater than that of the inverse of the absorption coefficient so that wavelengths at the higher end of the spectrum also can be absorbed [2]. Also the diffusion lengths must be larger than the film thickness in order to enhance the proper collection of the photo-generated carriers.

Various materials based on the above specification have been decided suitable for the thin films. The major areas of research have been with amorphous silicon, CIGS (Copper-Indium-Gallium-Selenium) and CdTe (Cadmium telluride). Their theoretical limits to efficiency are as shown in Figure 8.
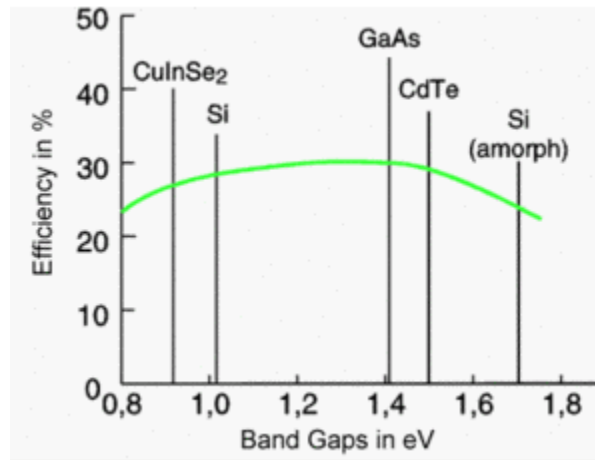
Figure 8 Limits to efficiency for different thin film materials [8]

I list below some of the major concerns that go into the selection of a material for thin film solar cells [2].

1. Direct band gap compatible for homo/hetero junctions

2. High optical absorption coefficient

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3. Possibility to produce p-type material for absorber and n-type for window layers.

4. Good lattice match

5. Good Electron affinities match with large band gap materials such as CdS so that low interface density states can be formed.

The confirmed efficiencies of some of the thin film solar cells are as listed in the following Table 1.

Table 1 Confirmed module terrestrial efficiencies measured under global AM1.5 spectrum (1000 W/m^2) at a cell temperature of 25 deg C (IEC 60904-3:2008 ASTM G-173-03 global) [9]

Classification[a]	Effic.[b] (%)	Area[c] (cm^2)	V_{oc} (V)	I_{sc} (A)	FF[d] (%)	Test centre (and date)	Description
Si (crystalline)	22.9 ± 0.6	778 (da)	5.60	3.97	80.3	Sandia (9/96)[e]	UNSW/Gochermann [34]
Si (large crystalline)	**21.4 ± 0.6**	**15780 (ap)**	**68.6**	**6.293**	**78.4**	**NREL (10/09)**	**SunPower [7]**
Si (multicrystalline)	**17.0 ± 0.2**	**8885 (ap)**	**22.67**	**8.86**	**75.0**	**ESTI (11/09)**	**ECN/REC (36 series cells) [8]**
Si (thin-film polycrystalline)	8.2 ± 0.2	661 (ap)	25.0	0.320	68.0	Sandia (7/02)[e]	Pacific Solar (1–2 μm on glass) [35]
CIGSS	13.5 ± 0.7	3459 (ap)	31.2	2.18	68.9	NREL (8/02)[e]	Showa Shell (Cd free) [36]
CdTe	10.9 ± 0.5	4874 (ap)	26.21	3.24	62.3	NREL (4/00)[e]	BP Solarex [37]
a-Si/a-SiGe/a-SiGe (tandem)[f]	10.4 ± 0.5[g]	905 (ap)	4.353	3.285	66.0	NREL (10/98)[e]	USSC [38]

[a] CIGSS, CuInGaSSe; a-Si, amorphous silicon/hydrogen alloy; a-SiGe, amorphous silicon/germanium/hydrogen alloy.
[b] Effic., efficiency.
[c] (ap), aperture area; (da), designated illumination area.
[d] FF, fill factor.
[e] Recalibrated from original measurement.
[f] Light soaked at NREL for 1000h at 50°C, nominally 1-sun illumination.
[g] Measured under IEC 60904-3 Ed. 1: 1989 reference spectrum.
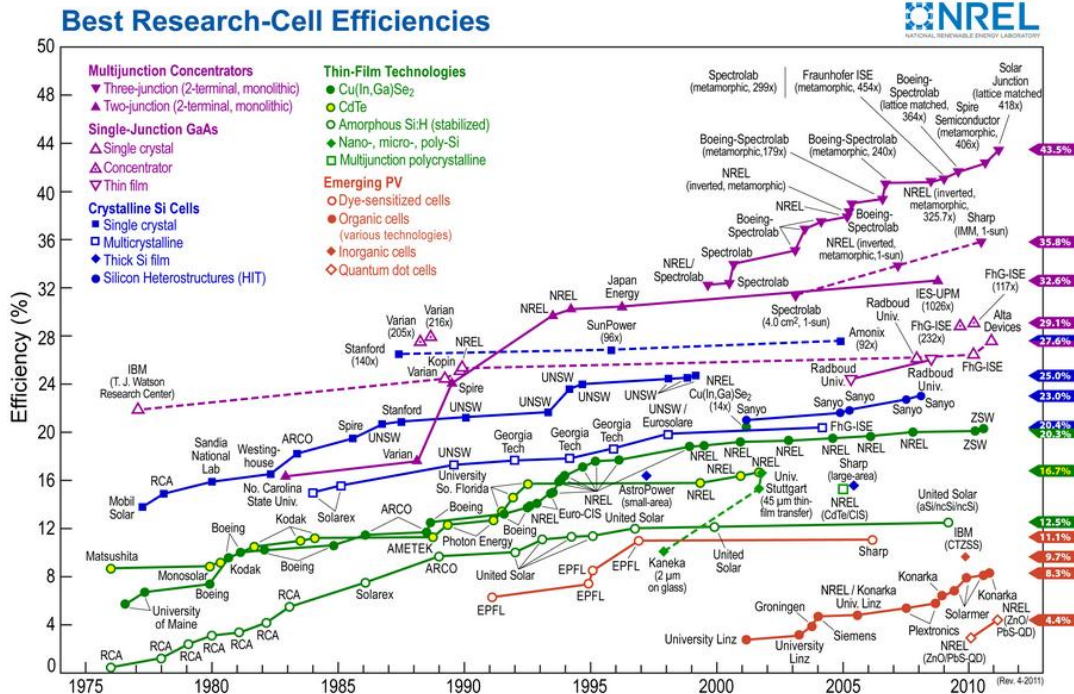
Figure 9 Best research solar cell efficiencies so far [9]

Figure 9 indicates the efficiency levels of different PV technologies so far at the research level. It has always been a challenge to reproduce them at large-scale manufacturing level. Issues about the CIGS will be discussed in the upcoming sections.

2.2   CIGS Thin Films

Evolution of CIGS (Copper Cu, Indium In, Gallium Ga, and Selenium Se) was from $CuInSe_2$ (CIS) thin films. CIGS belongs to chalcopyrite family. The CIS thin films were first to be studied in this family. CIS is a ternary compound with the energy band gap of about 1.0 eV. Such solar cells were fabricated with a structure having SLG (Soda Lime Glass)/Molybdenum layer (back contact)/CIS (Absorber)/CdS (Window)/ZnO (Front contact).CIS being the p-type and CdS being the n-type to form heterojunction.

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The CIS chalcopyrite structure is a diamond lattice with FCC tetragonal unit cell and is as shown in Figure 10.
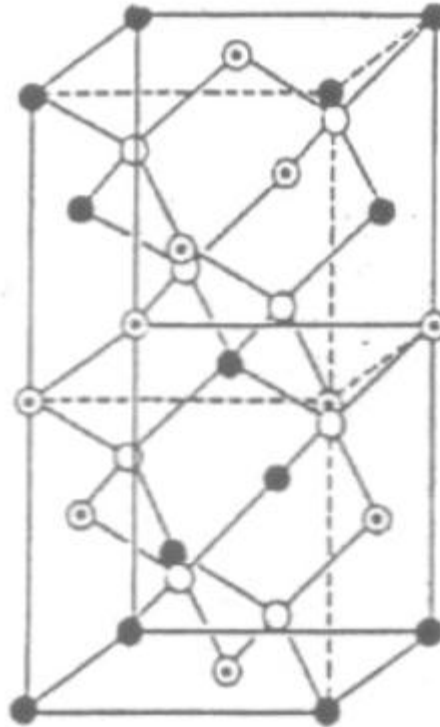
Figure 10 Chalcopyrite structure of CIS [10]

As mentioned the thin films are bound to have lattice defects, CIS had few of them. The major acceptor defects included that of Cu vacancies and Cu on In antisite defects. The major donor defects were that of In on Cu antisite defects and Se vacancies. During the course of CIS research by several people different things were dealt with, such as increasing the Copper level compared to Indium which made it more p-type conductive. This did not do any good as it led to the shorting of the junction due to excessive copper selenide formation. Such a problem could have been avoided by increasing the Indium level but this led to higher compensation effect. However CIS

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yielded better efficiencies comparatively it had lower V_{OC} s'[3]. This is when the idea of adding gallium to CIS came up and ultimately it evolved to CIGS [3]. The inclusion of gallium made it a quaternary semiconductor with a band gap of about 1.7eV. However the band gap variation for $CuIn_{(1-x)}Ga_xSe_2$ is represented by the Equation 12.

$$E_g = 1.011 + .664x + .249x(1-x)$$

Equation 12 Band gap variation in CIGS [3]

The incorporation of Ga increases the adhesion to molybdenum and hence changes a lot with regards to the defect mechanisms and film morphology. The Ga variation in the absorber layer can be done and is referred to as Ga grading which ultimately leads to enhanced collection of carriers by building up better quasi-electric fields. The grading is the phenomenon where a predominant shift in conduction bands takes place. It is as shown in Figure 11.

(a)   (b)
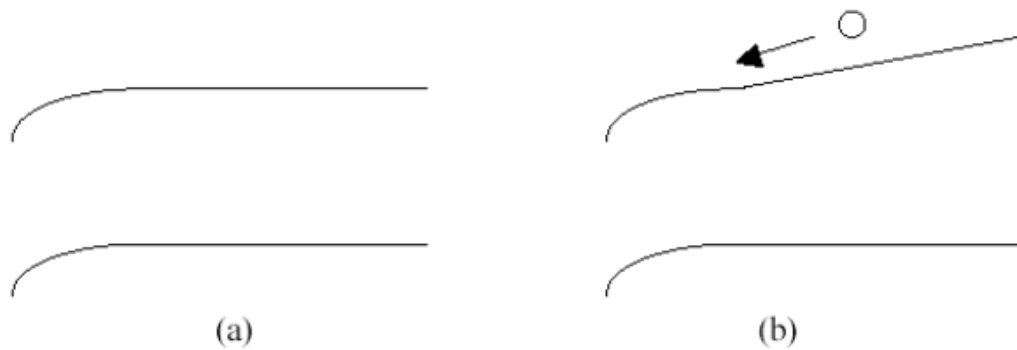
Figure 11 Band bending a)Without grading b)With grading [3]

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2.3 Role of Sodium in CIGS

Sodium is supplied from the SLG that we use as the substrate to make our solar cell. Sodium diffuses all the way through molybdenum from the glass and into the active semiconductor absorber. This changes several device properties such as conversion efficiencies [11], grain size, preferential orientation [12] and a reduced sensitivity of devices to the metal ratio [13].

Different models suggest mechanisms by which Na does this, they are:

1. Zhang/ Wei/ Zunger defect pair model: This model suggests the Na replaces few of the Cu vacancies thus reducing the defect pair formations [14]. As a result of this the hole density is affected and hence the device produces better VOC s' and FFs'.

2. Na acts as a catalyst in passivation of the selenium vacancies by oxygen [16].

3. Neumann defect pair model: Na substitutes Cu in the lattice reducing the cation disorder due to which there is an increase in VOC s' and FFs' [15].

2.4 Commercialization Issues

It was reported that the energy consumed in manufacturing in CIGS modules was 11 MJ/W_p which was the lowest for any of the existing PV technology [21]. Though thin film CIGS research boasts of proven 20% efficiencies at the lab scale [5] it is yet to be highly commercialized on a large scale. Since my thesis deals with the vacuum deposition of CIGS I would be focusing the problems caused by this. Issues are mainly due to Selenium. Being a very volatile substance the problems due to Se are more than one. A CIGS Manufacturer is constantly faced with Se build up in the reactors. Hence there is a necessity of frequent cleanup which eats away the time to manufacture the modules. Also due to the fact that excessive Se is required to grow stoichiometric films

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such a problem cannot be avoided as co-deposition is the major deposition technique used. Material properties of Se also play a considerable role in creating problems. Selenium has a very low sticking coefficient to the film growth surface [5] and also exhibits tendency to form chains and rings. Lot can be attributed to the kinetics and thermodynamics of the surface interactions. All these issues drive us to find a replacement to co-deposition technique. Thus was introduced the 2-step and 3-step CIGS. But even these methods have co-deposition as their deposition technique. It is important to remind the reader that in case of vacuum based CIGS a manufacturer always prefers metals being deposited first followed by their selenization due to the above discussed issues. Such issues form the basis of this thesis as we try to find a replacement for the co-deposition technique and also use it for a large-scale purpose. This thesis will explain to you a recipe that is made keeping all these in mind. Not to forget to add the issues of material utilization and growth mechanisms which were also under consideration.

2.5   Different Multi-Step CIGS Techniques Practiced in Vacuum Deposition

In this section am going to introduce several selenization techniques in vacuum deposition of the CIGS absorber that have been already found in order to tackle the issues with Se. Some of them are,

1. Selenization of stacks of metals and compound precursors [18]: A study conducted by F.B.Dejene to CIS (Copper-Indium-Selenium) and CIGS by selenization of stacks of metals and compound precursors by Se vapor [18]. In order to form the CuInSe2 absorber stacks of InSe /Cu/InSe were deposited on glass/Mo substrate at 200°C.Care was taken to see to that each of the precursors were deposited at identical conditions so that Mo had minimal influence on the films. In order to make Cu (In, Ga) Se2, the GaSe layers were

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deposited at around 300°C. In the CIGS thin films it was noted to have the ratios Cu/ (In+Ga) ~ 0.9 where Ga/ (Ga+In) was varied based on the GaSe deposition. Once the precursor films were done it was reacted with elemental Se vapor at 550°C for 60min. Hence single phase Cu (In, Ga) Se2 was produced by varying the deposition temperature of GaSe at the precursor step. So this made it easy to have variations with the lattice parameters of the chalcopyrite structure by just varying the Ga incorporation. SEM studies during the research indicated the crystalline qualities of these thin films were influenced by the Ga concentration in the bulk of the film. Later depositions of 50nm thick CdS buffer layer, 50nm of highly resistive intrinsic ZnO layer followed by 500nm of highly doped n-type ZnO were made to make complete devices. Such devices gave VOCs' in the range of 300-410mV, current densities Jscs' in the range of 25-35 mA/cm2 & fill factors (FFs') between 40-60%.

2. Sputtering and selenization [19]: The other method is where a novel absorber was made with the help of sputtering which was majorly used due to its uniformity over large area. The sputtering targets of Cu, In2Se3 and Ga2Se3 where used for this purpose. Two approaches were basically used to make quality CIGS films. In the first case initially a CIS layer without any spurious phases was selenized at a temperature of 520-530°C. On top of this a Ga2Se3 layer of .2-.4μmwas deposited to be finished of with a Cu layer on this. Later this film was selenized to form CIGS films. Smaller grain sizes and their tendency to coalesce were observed. Such devices on completion yielded VOCs' of 520-580mV,JSCs' of 32-34mA/cm2 and fill factors of 70-72%.A second approach were layers of In2Se3 ,Ga2Se3 and Cu were sputtered onto Moly. The In2Se3 & Ga2Se3 where deposited at a substrate temperature 350°C where as the Cu layer was sputtered at

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450°C. Such a Cu layer is said to have helped in the mixing up of the layers. Later this film was selenized at 530°C to get CIGS films.

2.6   New Trends

Companies such as Centrotherm photovoltaic AG in Germany and Showa Shell in Japan tend use the technique similar to the one mentioned in section 2.5 for production of their modules [19]. NREL promotes the three stage co-evaporation and has recorded an efficiency of 19.4% w.r.t it [21]. This is the elemental evaporation from point sources. But this technique over a large area cells has its own disadvantages. They propose a copper rich film at the end of the second stage which aids grain growth resulting in better morphologies and devices. Energy photovoltaics Inc uses elemental Se for CIGS purpose which makes it less toxic as compared to the use of H_2Se.They term their process as the hybrid process. In such a process an $(In_xGa_{1-x})_2Se_3$ layer was formed on heated substrate with In, Ga and Se. Then a Cu layer was stacked onto it then was selenized under a Se atmosphere. Later In, Ga and Se were supplied to finish as CIGS films. From different methods explained in this section and previous section we can see how important it is to have a control over different temperature profiles and growth mechanisms to have a control in order to produce quality CIGS. Not only this, efforts are also being made to find a better way to make the CdS layer onto the CIGS which completes the junction, ALD (Atomic Layer Deposition) is being suggested. Also reactive sputtering for the window layers of AlZnO are being suggested for better conductivity and IR transmission. Successful module fabrication with the CIGS thin films presently are faced with these key challenges [21]:

1. Uniform CIGS layer over a large area.

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2. Process control and its reproducibility.

3. A proper ZnO layer.

4. Scribing processes.

5. Interconnect resistance of ZnO/Mo interface.

The above issues have been driving factors on our evolution of a novel process for CIGS absorber for large-scale manufacturing. Once the intended pilot line is at full operation at USF it would be appropriate to deal with the other layers and right now we are focusing on the absorber at the lab scale.

CHAPTER 3   DEVICE STRUCTURE AND FABRICATION

In this section I am going to introduce to you the device structure of the solar cells I fabricated during the course of my thesis work, also different methodologies and deposition techniques used in the fabrication.

3.1   Device Structure
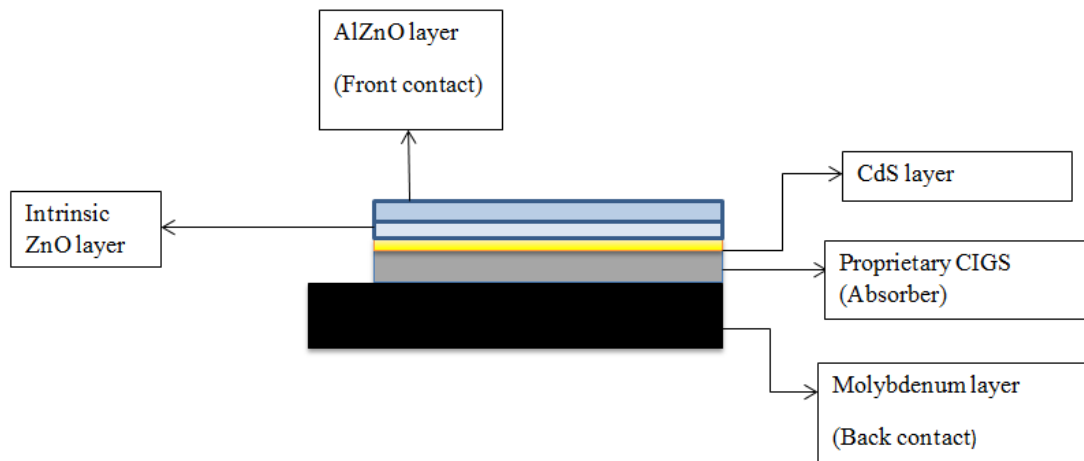
Figure 12 Device structure of the fabricated CIGS solar cell

The order of deposition for the fabrication of the Novel 2SSS CIGS thin film solar cell included that of

1. A bi-layer of Molybdenum as the back contact of 10kA° thickness by DC magnetron sputtering

2. The proprietary CIGS absorber on the molybdenum of about 2-2.5µm thickness by thermal evaporation

3. Followed by a 500A° thick CdS layer by chemical bath deposition (CBD) as the window layer

4. Then a 850A° thick intrinsic resistive ZnO layer by RF sputtering in the presence of Oxygen

5. Followed by Aluminum doped ZnO of 1500A° thick as the front contact by RF sputtering.

3.2   Fabrication

3.2.1   Substrate Cleaning

Two types of glass substrates were used during the course of this research work. The first type was corning 7059 glass of size 1.45" x 1.32" and 0.7mm thick was used for stoichiometric analysis of the novel absorber layer .This glass substrate was initially exposed running De-ionized(D.I) water , while it was brushed away using a dedicated brush used to clean substrates. Brushing was unidirectional and facing away from the glass so that the effects on the substrate due to cleaning remain constant throughout. This was done for about 45 seconds. Later the glass substrate was dropped into a Teflon beaker containing 10% diluted hydrofluoric (HF) acid for 5 seconds. Then the glass substrate was picked up from the beaker using Teflon tweezers and was exposed running D.I water to rinse off the HF for the next 25 seconds. After this in a quick succession of 3 seconds the substrate was again dipped in HF and removed to rinse it off with D.I water. After about 45 seconds the substrate was blown dry using compressed nitrogen. The second type of glass substrate that I used was that of soda lime glass (SLG) which was used to make devices. SLG was cut into size using a glass cutter. Later was washed under

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running D.I water and also brushed with normal soap. After complete rinse off under the D.I water, the glass pieces were then transferred to a holder in a beaker and then ultra-sonicated with 2-propanol for 30 mins. Then the 2-propanol was thrown away and the glass pieces were rinsed off with D.I water .The beaker was then filled with D.I water and ultra-sonicated it for 30 mins. Then SLG was left in the D.I water inside the beaker and whenever it was necessary they were picked up and exposed to running D.I water and dried under a nitrogen blow before use.

3.2.2 Molybdenum Deposition

A bi-layer of Molybdenum was deposited so that the absorber sticks on better to it. Bi-layer refers to moly being deposited at two different pressures to get a high/low resistive layers, as it is proved the adhesion of moly was better when such a practice was followed [3]. The first layer is deposited at a rate of 10A/s while the pressure inside the sputtering chamber being $5x10^{-3}$ Torr with DC power rating of 755W for 3 mins and 20 s. The second layer was deposited at a rate of 10A/s but at a pressure of $3x10^{-3}$ Torr inside the sputtering with a DC power rating of 755W for 13 mins and 14 s. Such a bi-layer acts as the back contact of the solar cell.

3.2.3 Absorber Layer

3.2.3.1 Bell Jar System

The absorber layer was deposited in a Bell jar system which is a Physical Vapor deposition system. The bell jar can be pumped down to vacuum with the help of mechanical pump initially, i.e. to a pressure of $1x10^{-2}$ Torr and then with the turbo pump

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to a pressure of $3x10^{-6}$ Torr at which we deposit CIGS absorber layer. It has 4 effusion cells each for Copper, Indium, Gallium and Selenium. Each effusion cell has a designated crystal sensor which monitors the rate of flux in A°/s of the source material emanating from the liner encapsulated with the crucibles sitting inside the effusion cells. These effusion cells are heated up with power controllers. The temperatures to which the thermal guns are heated are noted on the monitor of the power controllers with the help of thermocouples connected to the bottom of each of the effusion cells. The Figure 13 below explains more about the system.

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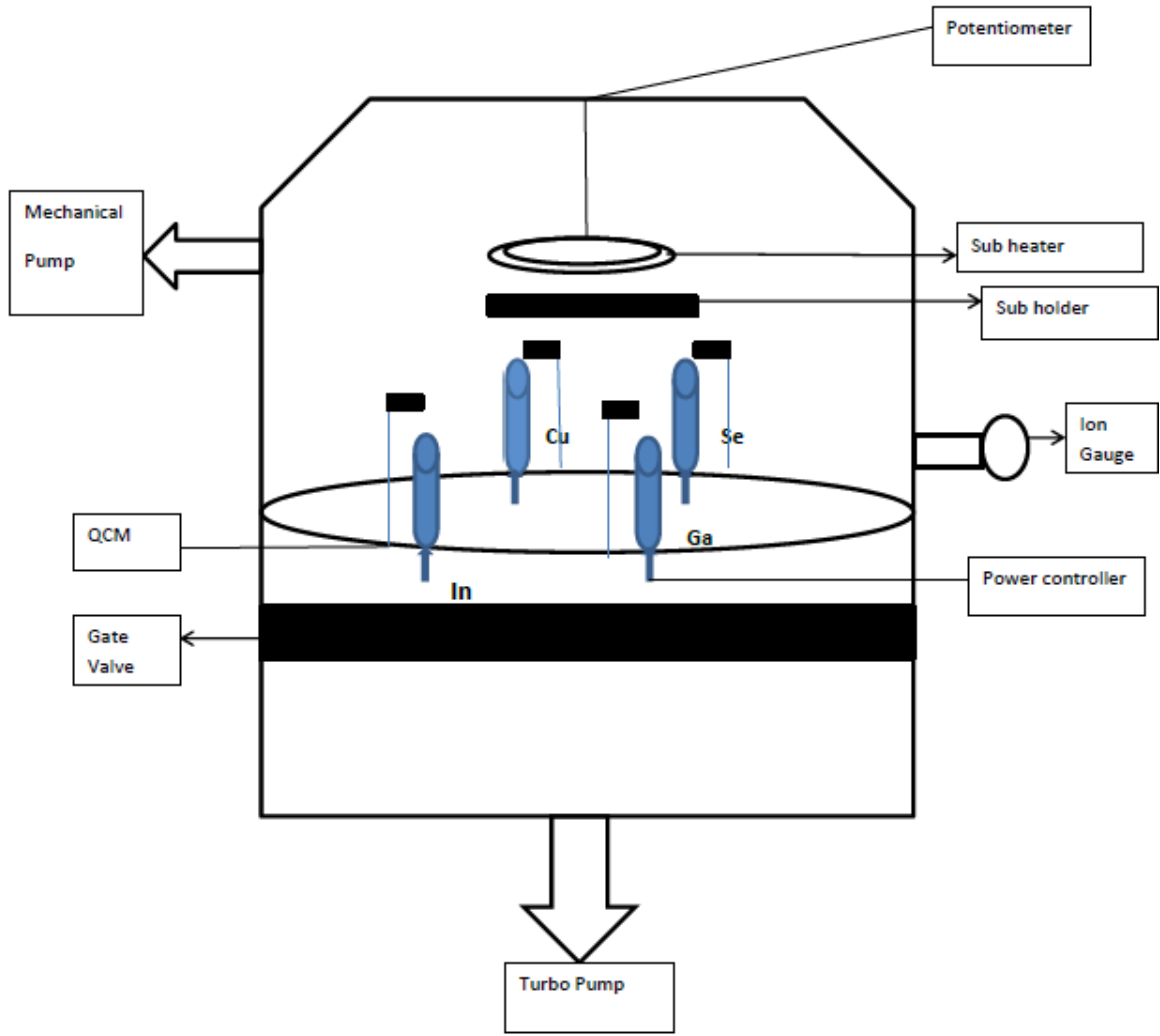
Figure 13 Bell jar system

It is also important to note the positioning of the effusion cells with regards to the substrate surface as shown in Figure 14. This is because we noticed certain variations in the device performance as the thickness of the absorber layer varied across the sample. This is discussed in detail in the results section.
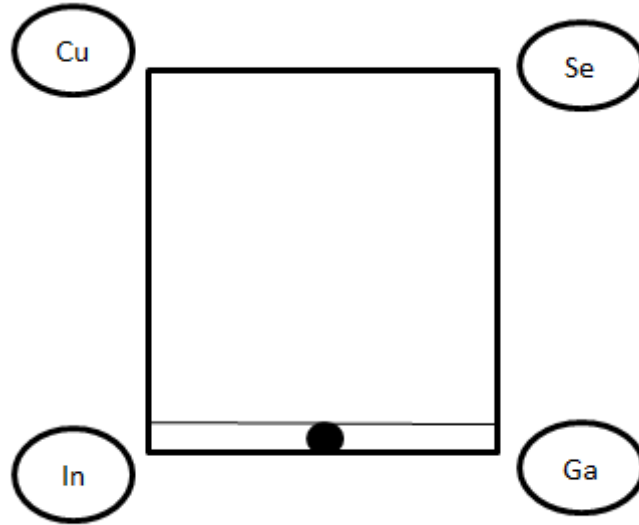
Figure 14 Effusion cells positioning with respect to the substrate surface

3.2.3.2 Thermal Evaporation Process

The thermal evaporation process is where the source material is heated to a temperature where the atoms leave the surface of the source and travel in a straight path until they reach another surface. So now the positioning of the source and substrate becomes an important factor along with the temperature of operation. Once the atoms reach another surface it would not re-evaporate as the vapor pressure is different at this surface hence would adhere to the surface. The thickness of such a deposition depends on the geometry of the source-substrate placements, time of evaporation and also the temperature of heat up.

3.2.3.3 Novel Absorber Layer

The heart of my thesis lies in this novel absorber layer. It is this layer where all photonic activities take place in a solar cell. Different solar cell types are named based on

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what goes into make this layer. We introduce to you a Novel approach to deposit this layer through this thesis.

The deposition of our absorber layer takes place in two stages. We name our process as 2SSS (2 Step Solid Selenization) which employs evaporated Se (solid) as the source of selenium. The base case for this approach is that in which the metals are deposited sequentially followed by the selenization step. Variations include deposition of metal selenides and all permutations of the order of deposition followed by selenization. First, a CGS (Copper-Gallium-Selenium) layer is deposited at a substrate temperature of 300°C.Though the sensor records a temperature of 300°C at the substrate it is believed to be typically 275°C at the substrate holder due to the spacing between the sample holder and substrate heater. So the initial layer is deposited for a time of 12.5 mins with fluxes of Cu@ 2A°/s, Ga@ 1.5A°/s and Se@15A°/s. It was noted the Cu/Ga ratio remained at the value of 1.2.Further details and the importance of these ratios are explained in the results section of the thesis. Once the CGS layer was finished depositing the metals where turned off with the Se left on while the substrate temperature was increased from 300°C-525°C(500°C at the substrate).There was time gap of 7-7.5 minutes for the temperature to rise from 275°C to 500°C as we were using a potentiometer for heat up. During this time the Selenium was left on at the same rate in order to prevent any loss of Ga from the film as Ga2Se was a volatile substance. The second step is to deposit a CIGS (Copper-Indium-Gallium-Selenium) layer. Once the substrate temperature was 500°C, the metals Cu, Ga and In was turned on at 2A/s, 1A/s and 2.5A/s flux rates respectively with Se at 15A/s for the next 25 mins. Then the metals were turned off and the Se was turned low to 5A/s while the potentiometer was switched off. But it took around 19 mins

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for the actual substrate temperature to drop from 500°C to 200°C, hence it is advisable for a cool down Se flux of 5A/s to be there in order to prevent In and Ga loss due to volatile species that were formed. This procedure explained is a more generalized one as there were few changes to it during the course of my thesis which will be explained better in the device results section. The substrate profile in Figure 15 shows the happenings during the absorber run.

Figure 15 Substrate profile

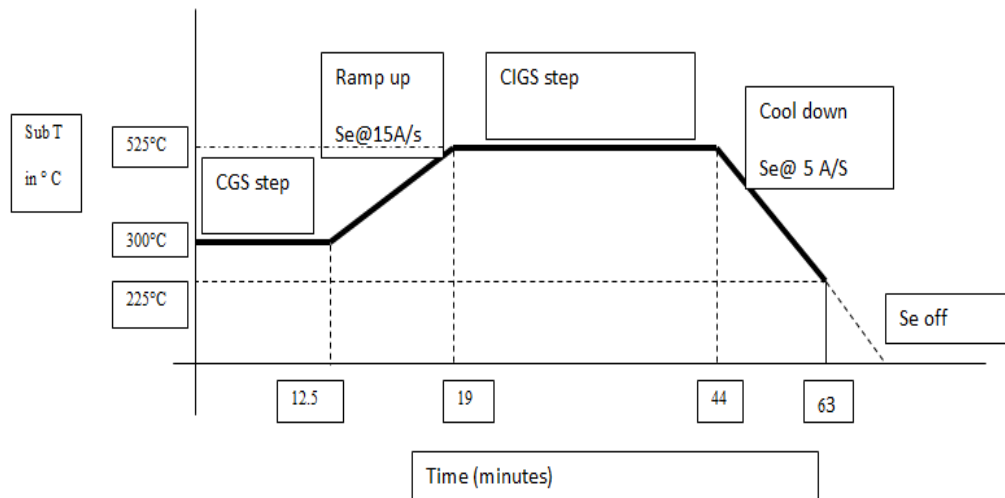### 3.2.4 Chemical Bath Deposition (Window Layer)

After the deposition of the absorber on Moly we move on to complete the CIGS junction by depositing the CdS (Cadmium Sulfide) layer of 300-500A° above it. The process we use to do so is called the chemical bath deposition (CBD).

The procedure is as follows. CBD is a solution based deposition. The four solutions that go into the process are

1. D.I water

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2. Strong Ammonia solution: I used the solution from Fischer Scientific.

3. Cadmium Acetate solution: 0.15M concentration of the same was made by dissolving 2.766g of the cadmium acetate salt in 800 ml D.I (De-Ionized)water and stirring it to clear solution with a magnetic stirrer.

4. Thiourea solution: 0.015M concentration of the same was made by dissolving 9.135g of thiourea salt in 800 ml D.I water and stirring it to clear solution with a magnetic stirrer.

We opted for 600ml based CBD for the devices made. A dedicated beaker, thermometer, custom made sample holder and a magnetic stirrer was maintained for the CBD purpose. Once I finished the CIGS deposition, after the cool down of the bell jar system the sample was taken out and placed on the custom made sample holder and immersed in 406ml of DI water in the beaker in which there was a thermometer and a magnetic stirrer already placed. The next step was to add 74.5 ml of strong ammonia solution and 59.6 ml of Cadmium acetate solution. This set up is then moved to a hotplate which was set to a predetermined heat level and speeds for the magnetic stirrer. When the mixture registered 30°C on the immersed thermometer, 59.6 ml of the .15M thiourea solution was poured into the beaker. The mixture was then heated to 80°C which is supposed to be the precipitation temperature. However when I was conducting the CBD process I found that the solution started turning yellow around 77°C, so I timed my run based on that. It is desirable to reduce the heat level on the hotplate once this temperature was reached so that the temperature of the mixture did not exceed 85°C. Based on my observations I made the depositions for around 3 minutes 5-15 seconds for all my devices before the mixture turned dark orange and precipitates formed. Once the deposition was finished the sample holder with the sample was picked up immediately and transferred to

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a clean beaker filled with D.I water and was allowed to cool down for about 2 minutes.Then the sample was exposed to running D.I water in order to remove anything sticking on the surface of the film and then blown dry using compressed nitrogen. The Figure 16 below explains the set up.
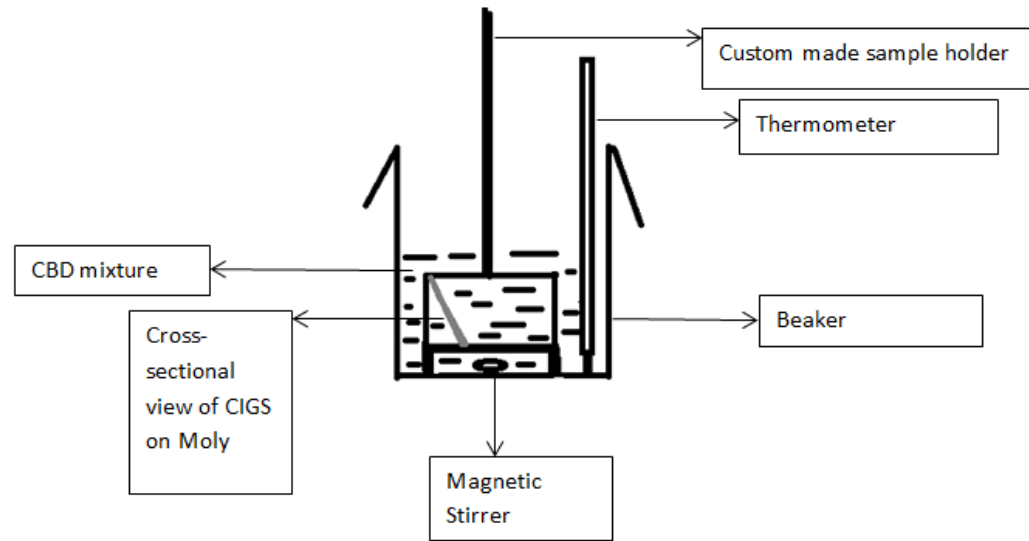
Figure 16 Chemical bath deposition apparatus

3.2.5 i-Zinc Oxide Sputter Deposition (Buffer Layer)

About 850A° of resistive intrinsic ZnO layer was deposited on the CdS layer using RF sputtering at a RF power of 175W. The substrate temperature was maintained at 125°C. The oxygen level was at 10% w.r.t argon. The i-ZnO was hitting the substrate at a rate of 1A/s.

3.2.6 AlZnO Sputter Deposition (Front Contact)

Aluminum doped ZnO acts as the front contact for the devices. It was RF sputtered onto the i-ZnO layer with a mask placed on it. The mask had about 10 dots of each area 1 cm^2.About 1500A° of it was deposited at a rate of 1A/s with the RF power at

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155W.The i-ZnO layer acts as the buffer layer which stops the Al from Al doped ZnO front contact from diffusing into the CdS layer and causing a short.

3.3   Characterization

3.3.1   Material Characterization

Though we know what material we are depositing sometimes we need to know how pure it is, whether there is any contamination. Apart from this it becomes very important to keep track of the stoichiometry or composition of the films that we are making as we make ample changes to the recipe throughout the course of this thesis work. EDS was the handiest tool for this purpose. EDS was extensively used when depositions were made on just the corning glass for determining the kinetics and thermodynamics of the CGS and the CIGS thin films in order to know the trade-offs between different elements going on. Also once the device fabrication stage was reached we had a practice of performing the EDS on the cell to be made at the stage where CdS was just finished depositing. Moly on soda lime glass, novel absorber on top of it with the layer of CdS for the junction this was the stage where EDS was done to monitor different ratios. Usually after CdS the sample is believed to behave more stable as it protects the surface from contamination. EDS was done at the maximum point of 25keV in order to consider the fact that maximum penetration of the electrons was achieved as it was important to know the accurate composition of the film. In such a case the first half micron of the absorber which is very important as far CIGS is concerned is under measurement.

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It is also important to mention that once the CGS and CIGS films were being made the XRD tool was also used to check the crystalline structure our absorber process was yielding otherwise of which the efforts to form a better process recipe would go in vain. Important results from XRD were found which are included in the results section.

3.3.2 Device Characterization

Once the solar cell was made it was subjected to an I-V test from which the response of the solar cell was found in the dark and the light.Corresponding plots have been explained and dealt with in the results section. Further a quantum efficiency test was also made on the solar cells. Necessary spectral response and transmission measurements were obtained from the spectrum analyzer.

CHAPTER 4   FILM GROWTH AND DEVICE RESULTS

4.1   Idea Behind the Process Recipe for Absorber Layer

Credit goes to around a decade's research in my lab over CIGS for the idea of a favorable process recipe for the large-scale manufacturing of the CIGS thin films. As explained previously a multistep process in which materials are deposited in different times about the deposition cycle are preferred over the conventional co-deposition method [20]. 2 step process for the absorber are of great interest. The proprietary process involves selenization from solid state Se. It involves deposition of metals in all possible permutations followed by sequential selenization [5] .The basic idea behind the 2-step process of depositing a CGS layer first and then a CIGS layer on top is due to the fact that a Cu-rich environment CGS layer provides a feasible platform for the growth of CIGS with larger grain size in the finished film.

4.2   Selenium Incorporation

Many issues related to kinetics and the thermodynamics can be attributed to the selenium incorporation methods used during the CIGS formation. It is a major concern of any CIGS deposition to have an appropriate substrate temperature found to selenize the film in order to get the desired properties. Hence we had to find out what was the feasible substrate temperature at which our metal precursors had to be selenized in order to get the stoichiometric films. The research on the CIGS film would be meaningless without

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figuring this out. Figure 17 indicates what we found out was desirable w.r.t to selenium incorporation in case of co-deposition.
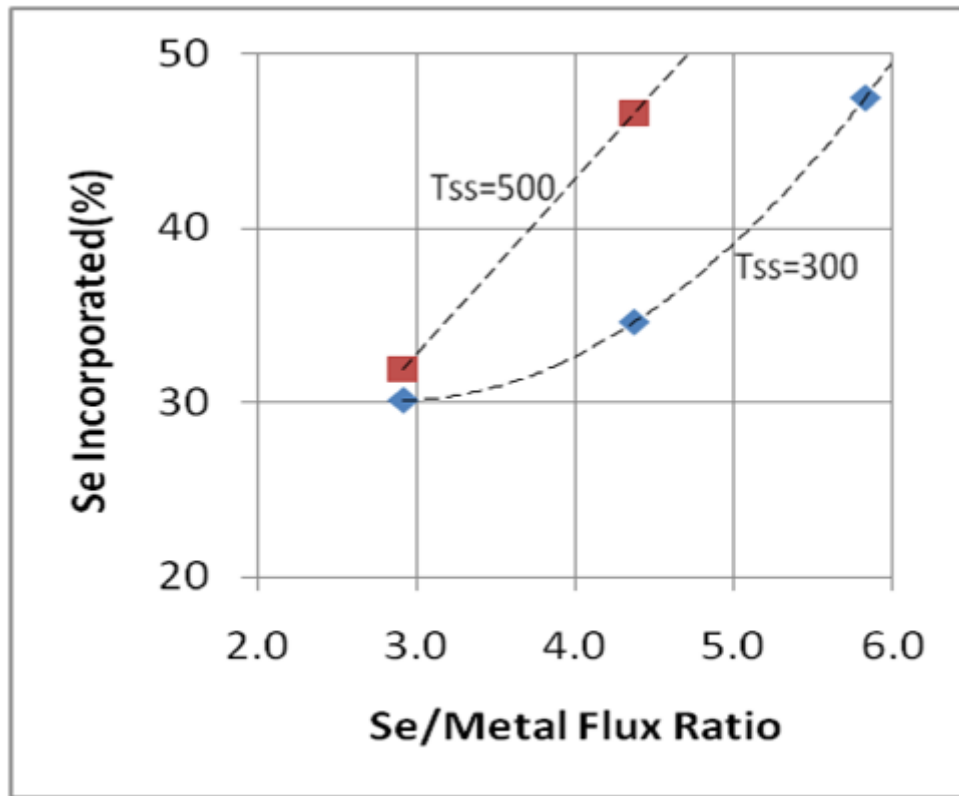
Figure 17 Selenium incorporated in co-deposited CIGS as a function of Se/metal flux ratio for two different substrate temperatures [5]

This becomes very important as vacuum deposition involves use of excessive selenium to get stoichiometric films. Whereas in the 2 step process we are using two different temperatures one being low at 300°C another around 550°C. It was found that increase in temperature helped enhanced incorporation of Se in the films for co-deposition. Such experiments were not done explicitly for the proprietary process used for 2-step depositions but other experiments were conducted to determine the selenization levels and are as explained in Figure 26. However the above data for single step or co-

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deposition process gives an idea how important the substrate temperature is for selenium incorporation.

4.3   Novel 2SSS Film Kinetics and Thermodynamics

It was very important for us to proceed in a step by step manner w.r.t finding out the right conditions for depositions of both the CGS layer and CIGS layer. This is because of certain material properties of the elements involved and their interesting inter-dependence. I was told this was the first time we had all the elements Cu, In, Ga and Se in one vacuum chamber in order for deposition. Our initial aim was to have a data base of all the growth kinetics going on w.r.t the new method as compared to the old methods of precursor selenization.

In order to do this we split the 2 steps separately and made a huge number of CGS and CIGS depositions with varied conditions to find a lot of things. I will explain these things in the coming sections. EDS was a very handy tool during this collection of the large amount of data.

4.3.1   CGS Step

The samples were made using the proprietary method on corning 7059 glass. Usually a deposition was made for 1000s at a substrate temperature of 300°C so that we could compare it to the 12.5 mins deposition that we intended to do in order to make devices. We had to also make sure the films were not very thin as the EDS would pick up the elements from the glass in such a case and would disturb our estimate of the proper stoichiometry. It was important for us to make co-deposition and also precursor selenization (PS) films in order to compare the results. It was also made sure that there

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was equivalent quantity of Cu, Ga and Se being deposited in each case. Figure 19 shows what we found out. The targeted composition was Cu/Ga of about 1.2 [5]. The co-deposited films attain the requisite Se of about 50%, but have Cu/Ga ratios of about 2.5 which indicate a Ga loss of about 50%. Needless to say this is substantial and of concern at a manufacturing level. At the other end of the range the precursor films have incorporated entire incident Ga, but are substantially low in Se content. Increasing the Se flux for the PS films can and does raise the Se content level [5]. Clearly there appears to be a tradeoff between Se and Ga incorporation. The proprietary films play into this tradeoff, and as can be seen fill the range between the co-deposition and PS endpoints. Calculations indicate there is just 33% loss of Ga whereas there is 50% loss of Ga in the co-deposited films. In the lower Cu/Ga range the proprietary films can also preserve all of the Ga while incorporating 35% Se relative to 25% for the PS films. So in terms of effective Ga and Se utilization these films are superior to both co-deposition and PS films. Loss of Ga would be because of formation of volatile species such as Ga_2Se.Our XRD results as shown in Figure 18 confirm that we are forming Cu_2Se and Ga_2Se_3 which does indicate that we have Cu and Ga in our films. There is no unreacted metal that shows up in the XRD result. Our tentative conclusion at present is that some XRD peaks are dependent on film stoichiometry and growth induced microstructure [5]. Gabor reports changes in the γ-Ga2Se3 $2\theta=37°$-$38°$ peak which practically disappears when Cu levels exceed 24% in CIGS [24]. We intend to pursue this matter further since these uncharted compositions may prove to be useful precursor films [5]. A different mechanism is involved and we are dissuading ourselves from forming volatile species. Further a study for Se incorporation targeted at 50% was conducted and the following

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results as shown in Figure 20 were obtained. It shows the effect of Se/metal flux level on

film composition. Figure 20 shows that there is no loss of Ga over a range of metal flux

ratios.
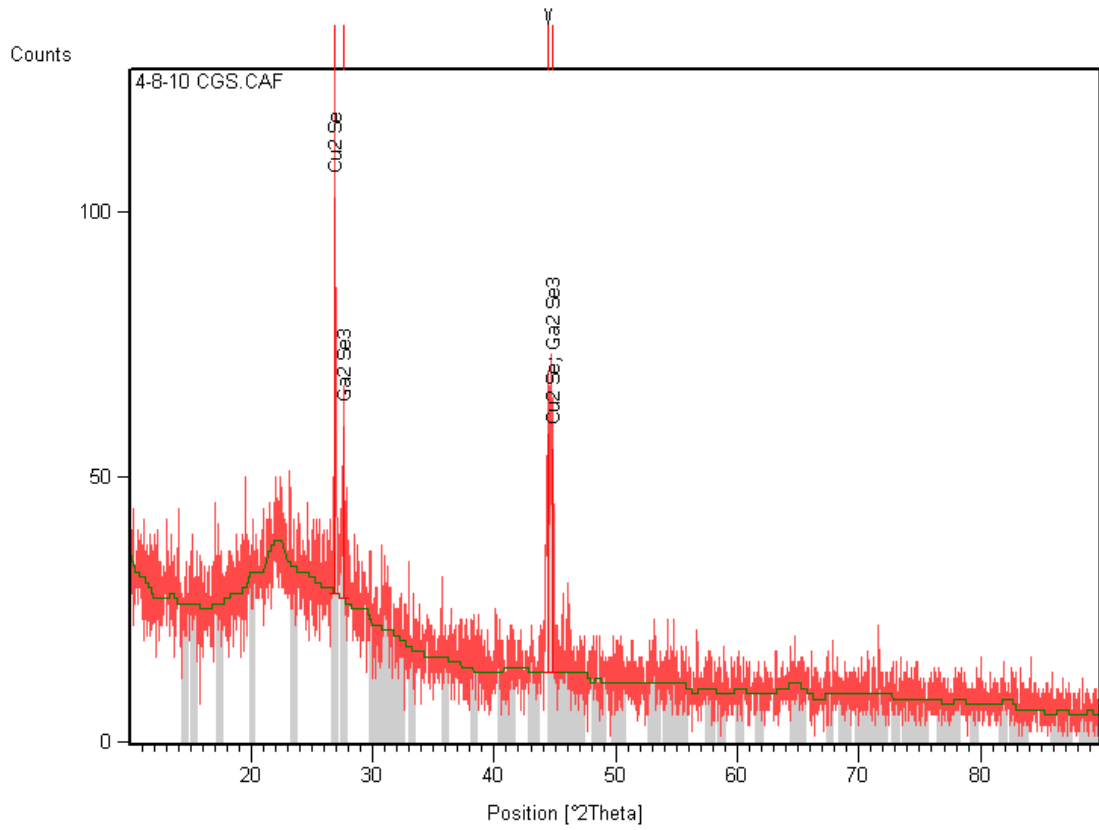
Figure 18 XRD of the novel 2SSS CGS film
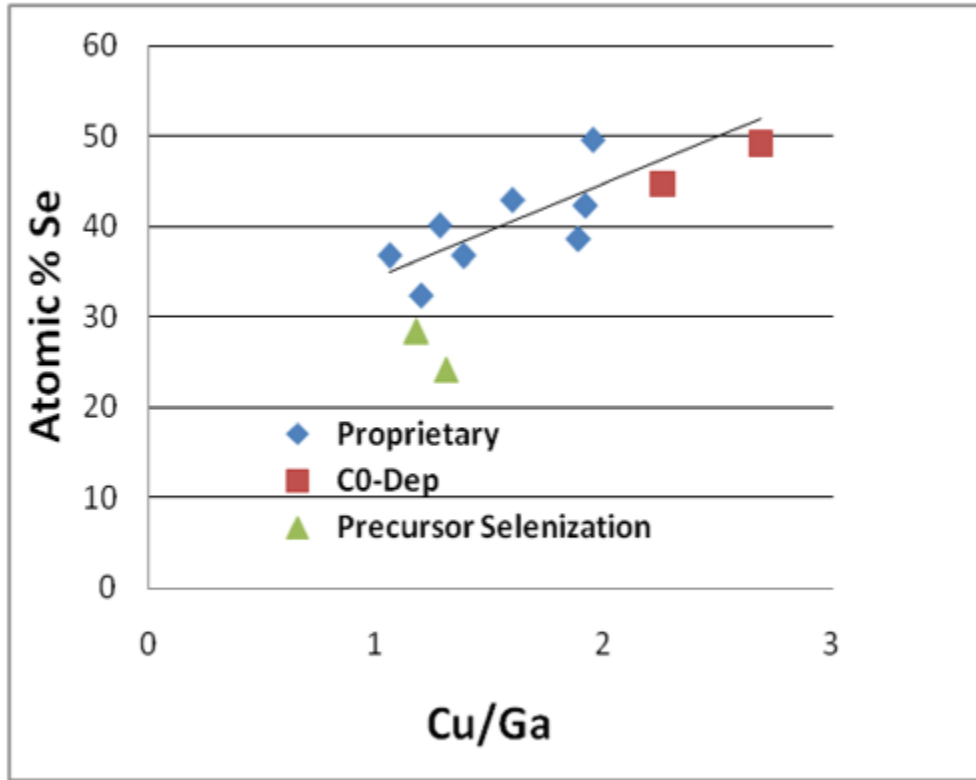
Figure 19 Se dependence on Cu/Ga for step 1 Cu rich 2SSS CGS films [5]
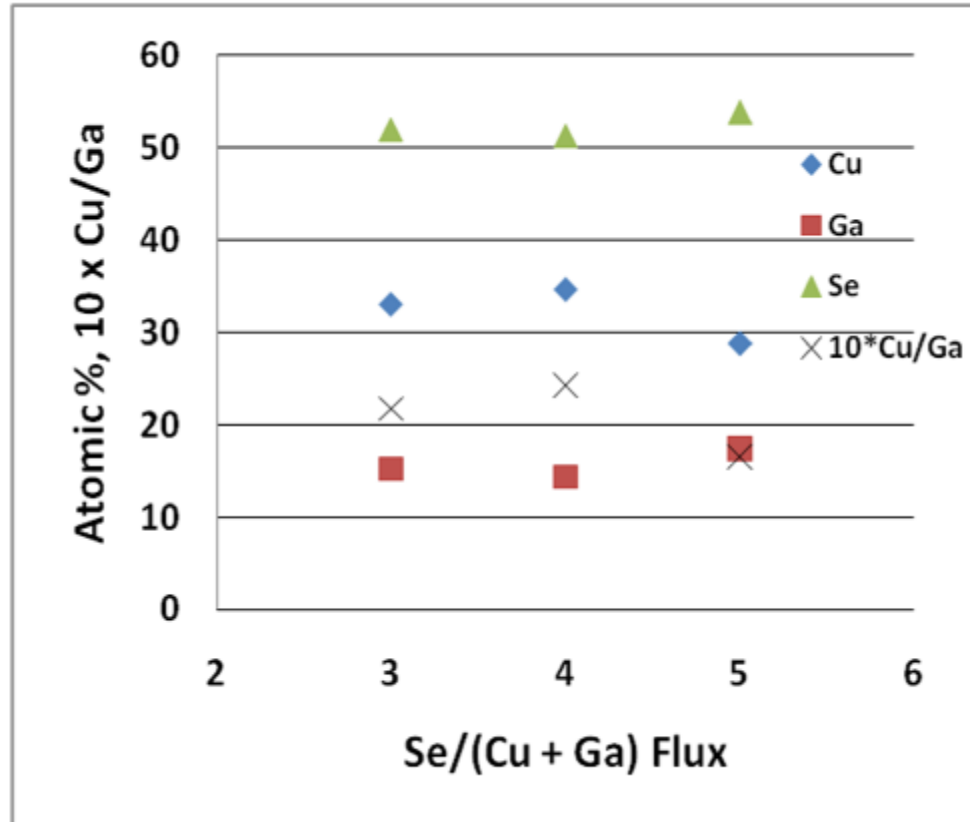
Figure 20 Atomic composition and Cu/Ga ratio as function of Se/metal flux for proprietary films [5]

4.3.2 Penetrating into the Film with EDS at Different Voltages

A study of 2SSS films and co-deposition films made with equal quantities of Se flux and deposition time was done. As shown in Figure 21 it was found that though the Cu/Ga ratio remains the same the selenization level was 27%. In order to get the desired ratio of near Cu/Ga =1.2 we had to further selenize the 2SSS film in Se flux for 30 mins at a substrate temperature of 300°C. This means additional Se flux and also Ga loss which is why Cu/Ga increases, the reason being more Se required to penetrate through the pre-cursor layers to fully selenize them. This fosters the condition to form volatile species. We developed a modified 2SSS process to overcome this problem.

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Figure 21 shows the comparison between standard 2SSS and modified 2SSS process with that of the co-deposition films.
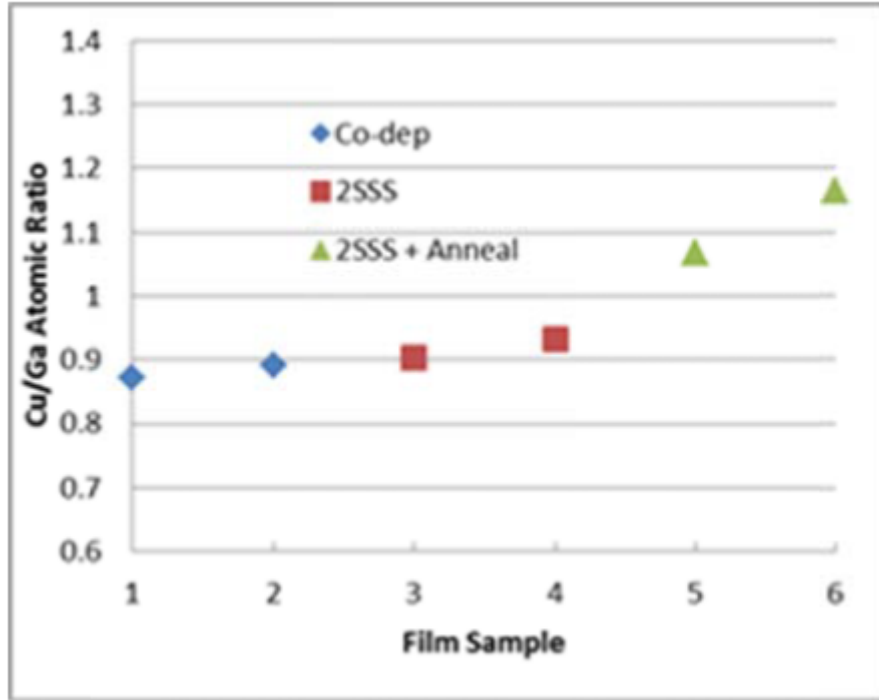
Figure 21 Cu/Ga variation in 2SSS and co-deposition films [6]

Selenization profiles of such films were obtained when different EDS beam voltages where used on them. A change in Se composition was observed. Care was taken to maintain the composition of the CGS film by our novel process is same as the one of co-deposition, which made us find the modified 2SSS process. One of the main reasons for this was the tendency of Ga to flow backwards in the film. Hence EDS measurements for each of the co-deposition, 2SSS process and modified 2SSS processes samples were taken at 15kV, 20kV and 25kV respectively. It is to be noted that at low beam voltages the ratios were manually computed by taking the peak amplitudes as the EDS algorithm may not give accurate atomic ratios. Figure 23, Figure 24 and Figure 25 just shows how

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atomic ratios varied under EDS at different beam voltages. This can be compared to depth profiling of thin film .Whatever was the effect on the films our goal was to achieve a composition similar to co-deposition. So you can see from the plot below we were able to achieve this with our modified 2SSS process.
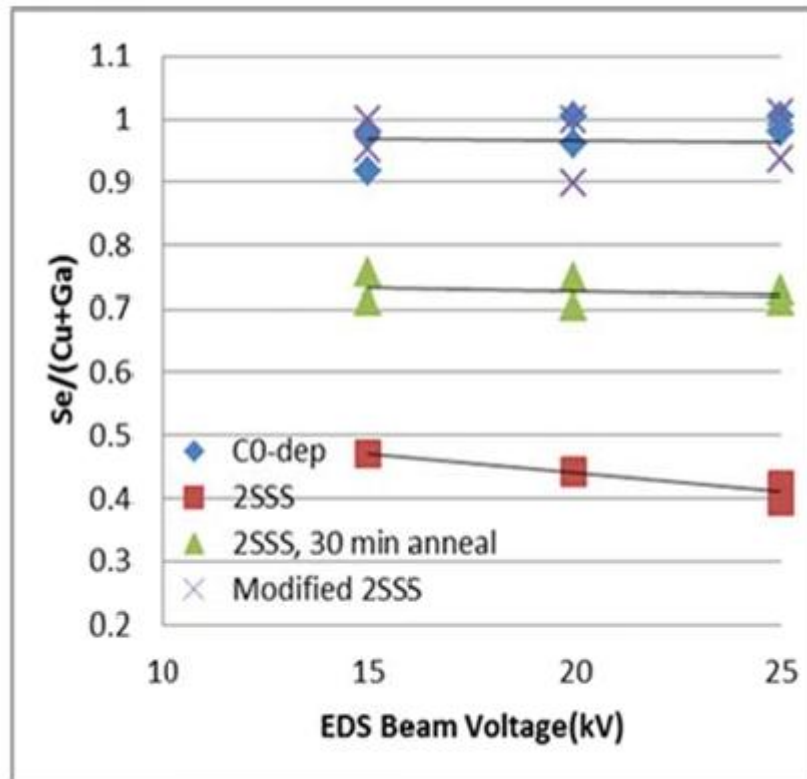
Figure 22 Se/metal ratio as a function of EDS beam voltage for CGS films made by co-deposition, 2SSS and modified 2SSS process [6]

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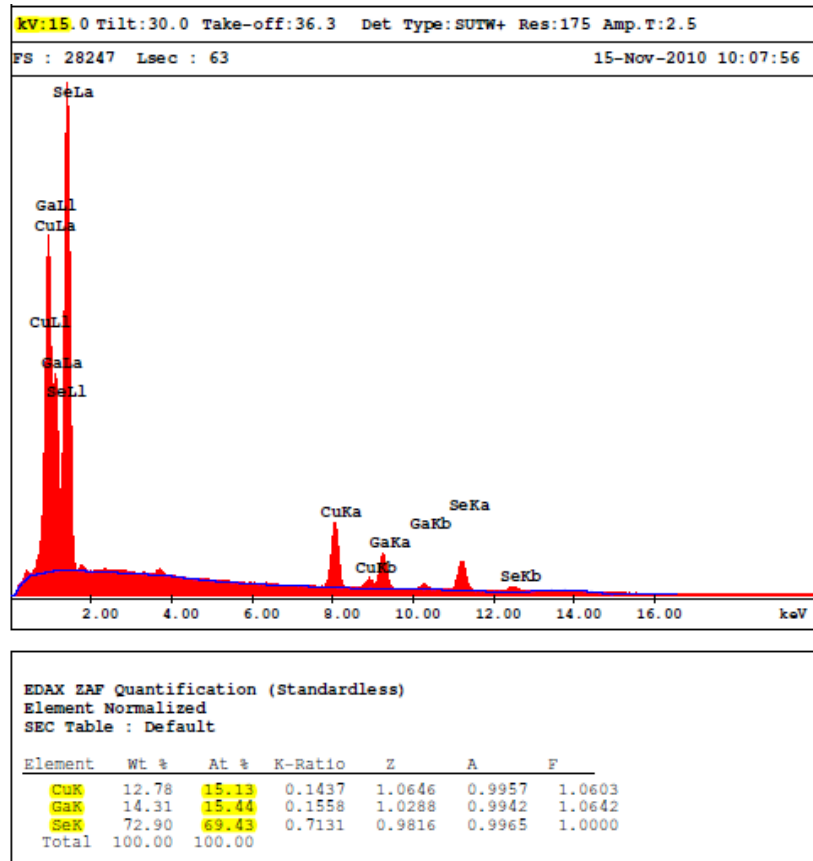
Figure 23 EDS on co-deposition CGS sample at 15kV
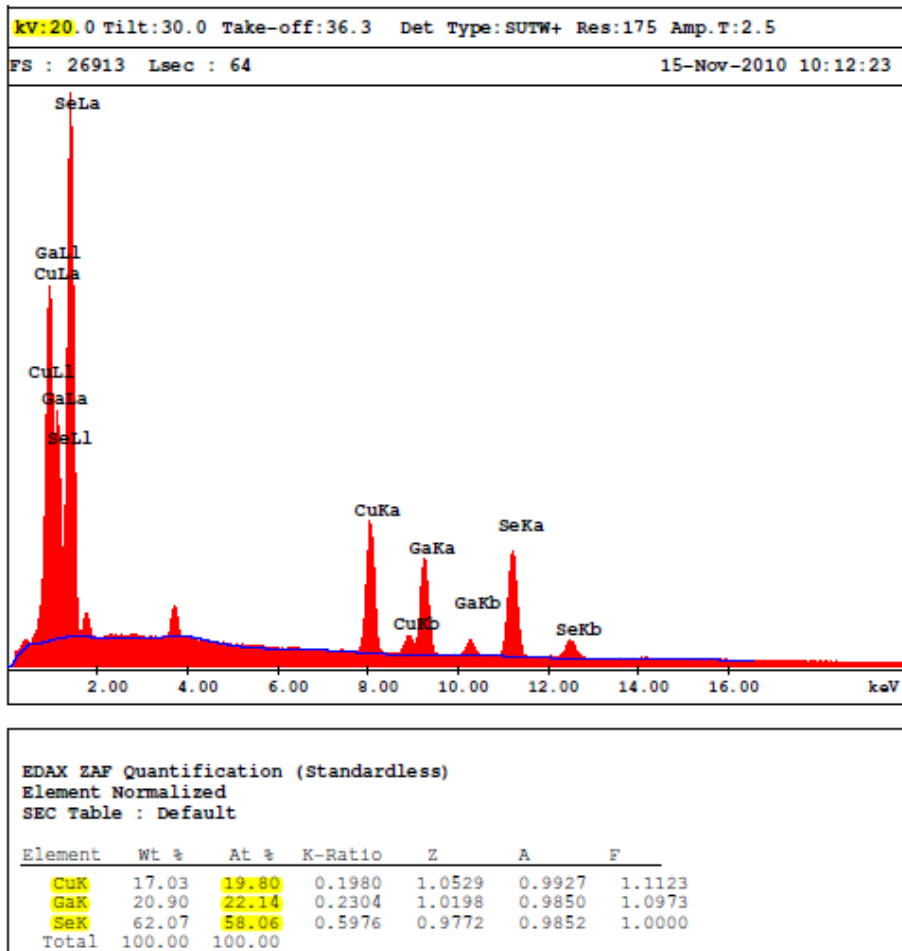
Figure 24 EDS on co-deposition CGS sample at 20kV
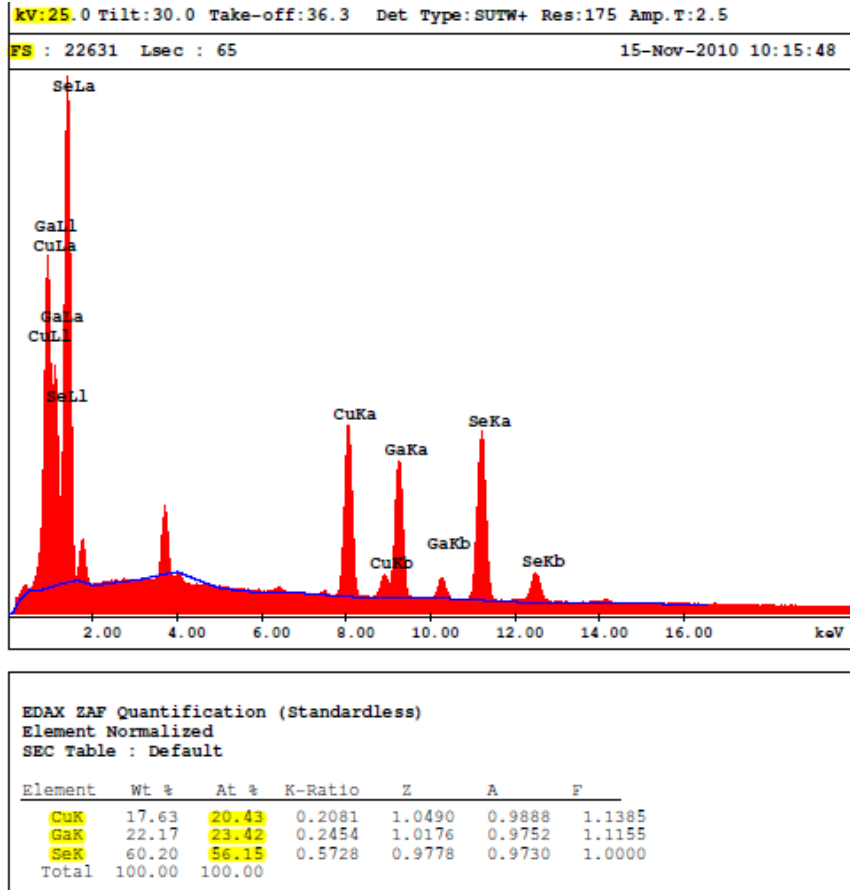
Figure 25 EDS on co-deposition CGS sample at 25kV

4.3.3 CIGS Step

After finding things in the first step we move onto the second step where we also introduce Indium into the film. Similar results were found, as even In has the tendency to form volatile species. Plot for Cu/Ga and Cu/In for different samples are as shown in the Figure 26. It is Cu/In and Cu/Ga variation as a function of Se content in 2step-2SSS CIGS films. An interdependency between Cu/In and Cu/Ga with selenization level was found but however we were able to produce films with full selenization without the loss of group III elements. The selenization percentage varied between 45-57% as shown in Figure 26. After proper analysis we find that the desirable stoichiometric ratios are $0.9 \leq$ Cu/ (In+Ga) ≤ 1 and $0.2 \leq$ Ga/ (Ga+In) ≤ 0.3.
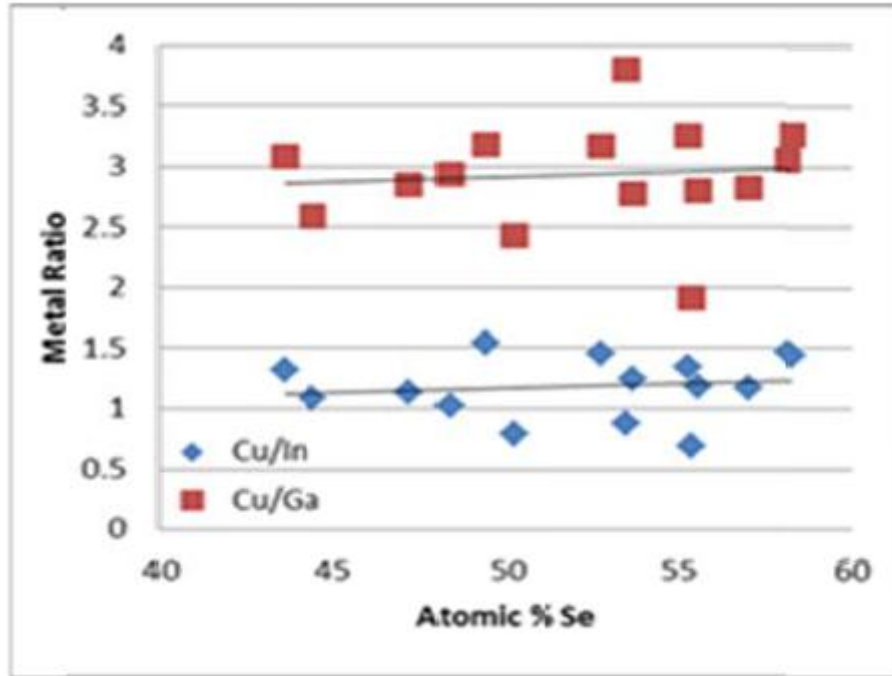
Figure 26 Cu/In and Cu/Ga ratio as a function of Se content in the 2 step 2SSS CIGS films [6]

4.4   Device Results

4.4.1   Few Changes to Process Recipe

There were changes to the process recipe of absorber made because of certain surface issues we were facing as we went into making devices on the whole (Solar cells).The changes included were

1. Raised the substrate temperature for the CIGS step to 550°C.This increased the reaction rates. This also helps the CGS layer to be in molten state and enhances the grain growth.

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2. Cu cut-off at the end of the CIGS step: Such a step was done to get the Cu/III ratio to desired ratio i.e. between 0.9-1.0.

3. We let Se source on for an extra 10 mins at the end of the CIGS step because the metals deposited at the end of the run required some more time to be selenized.

4.4.2   Thickness Variation

During the course of the research we had to replace several of the effusion cells partially and completely due to different reasons of shorting, meltdowns etc., during which the orientation of the thermal guns might have been changed. As explained in section 3.2.3.1 the positions of these point sources are important. However this gave rise to a thickness variation of the absorber layer w.r.t the positions of the thermal guns .In order to keep track of these thickness variations depositions were made on 7059 corning glass which was taped with a special polymer tape for the Dektek measurements. Similar 15 spots were measured on each elemental deposition made on the 7059 glass. Since the measurement of Ga and In variations cannot be observed with them individually over the glass sample, they were deposited along with copper. It is represented in the following plot in Figure 27.

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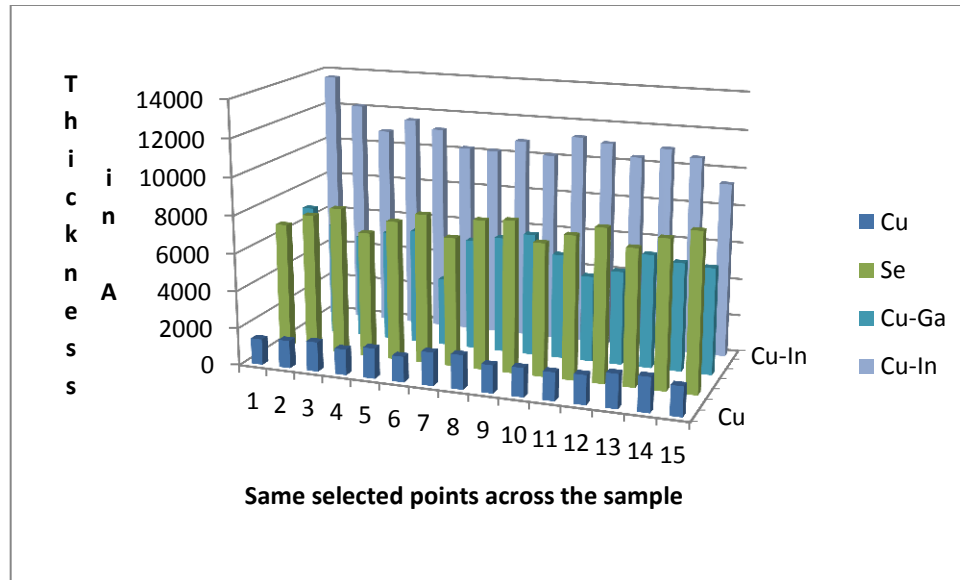
Figure 27 Thickness variation across the sample due to effusion cell orientations

These thickness variations were kept in mind when devices were being made so as to correlate our EDS data and device results (such as V_{oc}, J_{sc} and FF) at various points on our solar cell device.

I would like to cite an example of how things were correlated actually. The EDS was measured across opposite diagonals of the sample which consisted total of 5 points on the sample after the CdS layer was deposited. We can also see how the parameters V_{oc}, J_{sc} and FF varied across the sample. The mask before depositing AlZnO was placed at an angle of 90º to the sample. To give the reader an idea, the comparisons of the results of a device SC32 as in Figure 28 shows this. The part A) explains the points where EDS was measured, B) gives the Cu/III ratio and Ga/III ratio of the device made w.r.t the positions of the effusion cells in the bell jar system and C) gives the device results.

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Se

	EDS	Cu				Cu		Device Properties			
Cu	18.02	19.47	Se					2	4	6	8
In	13.32	12.82									
Ga	7.54	6.03					Jsc	23.9	24.98	26.26	28.01
Se	53.65	52.35	Cu/III	0.86385	1.03289		Voc	430	480	530	450
Cd	3.05	4.1	Ga/III	0.36146	0.31989		FF	0.282	0.314	0.458	0.37
S	4.41	5.22			0.85118						
	17.73				0.3471			21.94	26.33	29.3	26.05
	13.6							470	520	530	510
	7.23			0.71605	0.83109			0.22	0.391	0.466	0.423
	54.27			0.36123	0.32772			1	3	5	7
	2.99		Ga			In					
	4.18						Jsc in mA/cm sq				
	15.66	17.27									
	13.97	13.97					Voc in milli volts				
	7.9	6.81									
	55.49	54.47									
	2.9	3.18									
	4.09	4.31									

Ga   In

All in atomic %

A)   B)   C)

Figure 28 Variations in the parameters of the device due to thickness variations

4.4.3 Co-Deposition Device Results

4.4.3.1 Device SC9

This device was made with absorber layer recipe as mentioned in section 3.2.3.3 with the only change being the substrate temperature was 550°C and not 525°C. This is for the reason explained in section 4.4.1. It is to be noted in the I-V curves the current densities (J) are calculated by multiplying a factor of 10 to the currents (I) as the areas of our devices are 0.1 cm^2.

4.4.3.2 I-V Results for Device SC9

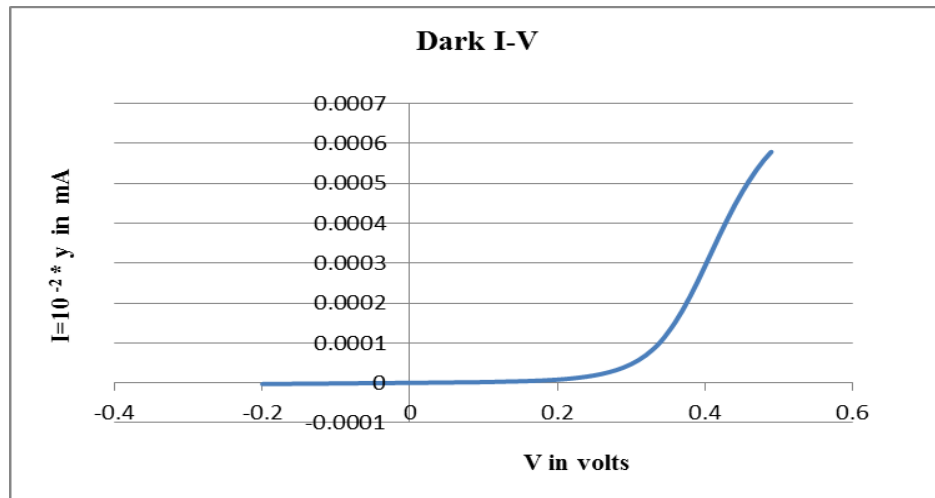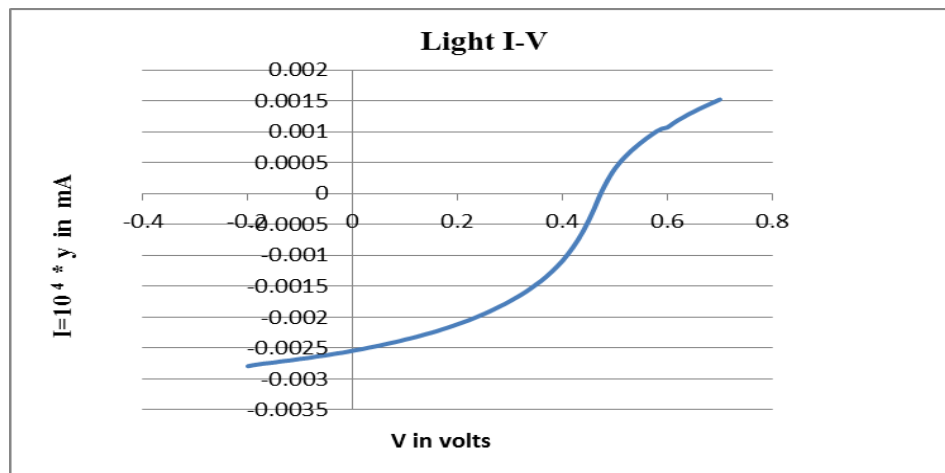**Figure 29 Dark I-V for device SC9**

Figure 30 Light I-V for device SC9

The dark current-voltage results indicate problems with the contacts. This co-deposition device had a front contact AlZnO deposited with the substrate not being heated to 125°C, which meant there was no proper diffusion of aluminum in ZnO. The light I-V indicated there could be another junction being formed and hence we had to

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calibrate our CdS layer better. Such changes were made and the next set of co-deposition devices was made.

4.4.3.3 Device SC32

This is a co-deposition device made with changes 1, 2 and 3 as mentioned in the section 4.4.1. It was very important to do the Cu cut-off at the end of CIGS step because this step ensured we got desired Cu/III ratio though it almost mimicked a 3-step process. The device results also improved compared to earlier devices such as SC9 as substrate was being heated during the front contact deposition and also the chemical bath deposition of CdS layer was better monitored now.

4.4.3.4 I-V Results for Device SC32

Dark I-V

Y-axis: I=10^{-2} * y in mA

Values: 0.0006, 0.0005, 0.0004, 0.0003, 0.0002, 0.0001, 0, -0.0001

X-axis: V in volts

Values: -0.4, -0.2, 0, 0.2, 0.4, 0.6, 0.8
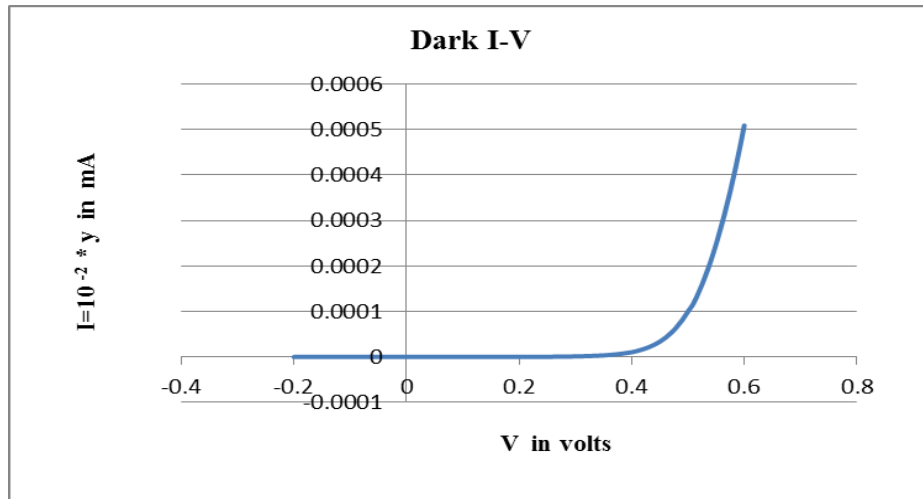
Figure 31 Dark I-V for device SC32

Light I-V

Y-axis: I = 10^{4} * y in mA

Values: 0.002, 0.001, 0, -0.001, -0.002, -0.003, -0.004

X-axis: V in volts

Values: -0.4, -0.2, 0, 0.2, 0.4, 0.6, 0.8

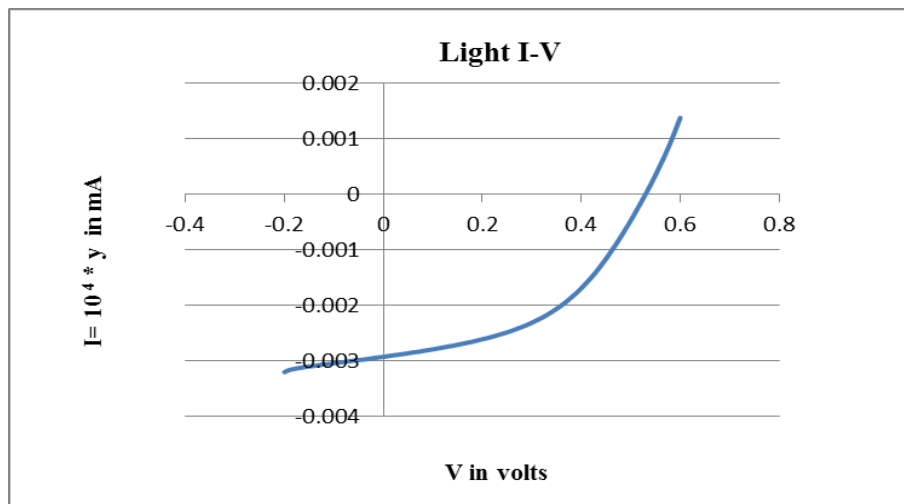**Figure 32 Light I-V for device SC32**

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4.5 Proprietary 2SSS Device Results

4.5.1 Device SC34

The process of making devices with novel process was started of initially with the process being used only in the CGS step of device making whereas the CIGS step was still a co-deposition process. We call these devices as the hybrid devices.SC34 is such a device where 2SSS process was used in the CGS step and CIGS step was a co-deposition. However all the changes to the process recipe in section 4.4.1 were still maintained as these had an impact on the device irrespective of whether co-deposition or 2SSS process were used.
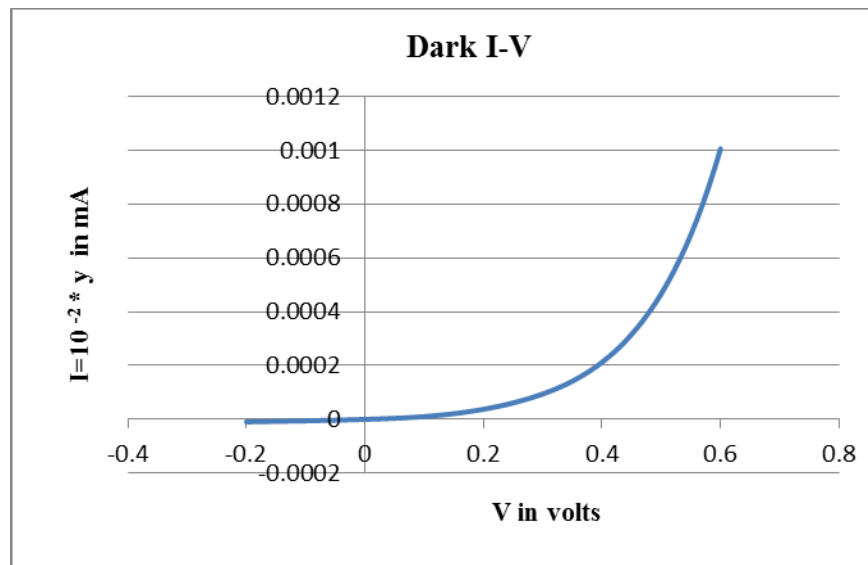
4.5.1.1 I-V Results for Device SC34

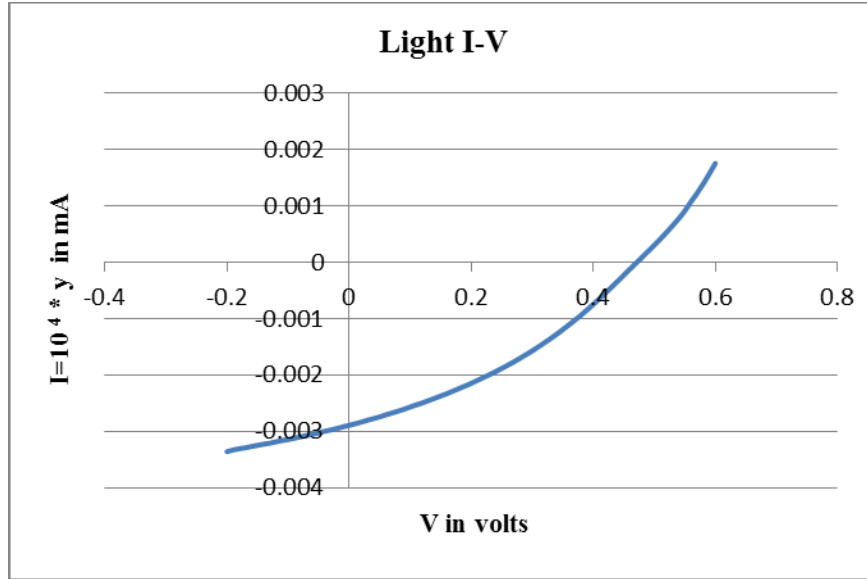**Figure 33 Dark I-V for device SC34**

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Figure 34 Light I-V for device SC34

On making comparisons with the reference co-deposition devices it was observed that the co-deposition devices had V_{oc}s' in the range of lower 500mV and J_{sc}s' near 30mA/cm^2. However the devices made with the novel 2SSS process had similar range of V_{oc}s', the J_{sc}s' in a lower 30mA/cm^2 range. This was interesting to take note of because though we were able to match the compositional and micro-structural properties of co-deposition there was something else going on with the devices made with 2SSS process. We sense this is something to do with the transport properties of the absorber considering the nature of our 2SSS process. It is to be noted that very minute differences in the point-defect level can have a large impact on the device performance. A proper measure of such properties would be through quantum efficiency (QE) measurements. So we proceed to do QE measurements, the results are discussed in the upcoming section.

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4.6   Quantum Efficiency Measurements

With the issue of lower $J_{sc}s'$ observed with the hybrid 2SSS devices it was necessary to make a comparison of its QE with that of co-deposition devices. The following Figure 35 gives the comparison of 2SSS device QEs' v/s co-deposition QEs'.
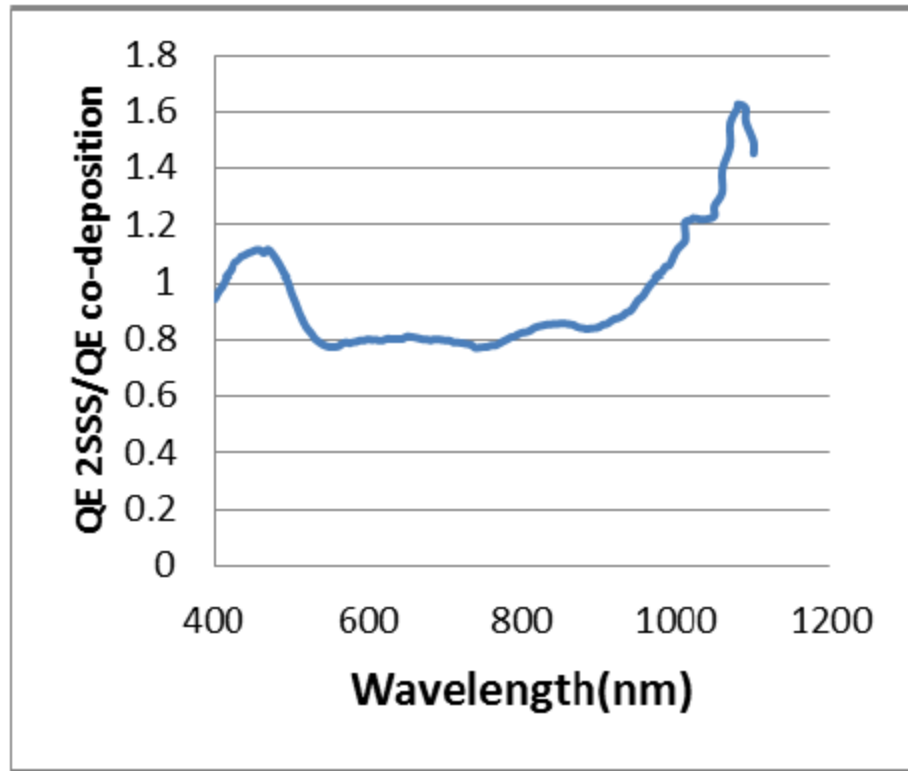
Figure 35 Quantum efficiency comparisons [6]

Overall it can be seen that quantum efficiencies of the hybrid devices was almost 80% of that of co-deposition QEs' made with the same conditions. However there can be seen higher quantum efficiency in the blue region of the spectrum by the 2SSS devices. The additional QE in the red region is attributed the band gap of the 2SSS films being lower comparatively to the co-deposition devices. This is surprising to have been exhibited by a device which is still largely deposited by co-deposition process in the

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CIGS step. Such observations might be as a result of less Ga being supplied to the space charge layer from the underlying CGS layer that is being deposited by 2SSS process. Further study of such complex mechanisms exhibited by Ga can lead us to making devices with excellent performances.

CHAPTER 5   CONCLUSIONS AND RECOMMENDATIONS

The newly found 2SSS process for the CIGS absorber can be successfully implemented for the large-scale manufacturing as there are fewer issues of selenium for the manufacturer. Though devices with results comparable to co-deposition were fabricated, better results can be achieved with controlled CdS deposition and tweaking up of the ZnO layers. The hybrid devices results obtained promises an excellent future for 2SSS process in the large-scale manufacturing level compared to co-deposition process overcoming the problems of improper selenium and gallium incorporation.

During the course of making devices one of the major problems that I faced included that of effusion cell failures. This led to change in their orientation and made it difficult for the composition of the absorber layer to be maintained. The procedure of maintaining the effusion cells having metals at a higher temperature compared to selenium when it is in use becomes very important so that there is no deposition of Se onto the thermal guns. Frequent sandblasting of the shields of the effusion cells is necessary so that metal-Se compounds formed sticking onto the surface do not diffuse through the copper turnings at the base and onto the heater leads and thermo-couple leads. A frequent check on the mechanical pump oil is a must as Se vapors tend to get into it and stop them from normal operation.

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I would also recommend a proper calibration of CdS layer can be achieved with the sample being picked up from the reaction solution right before the precipitates are formed. This is quite tricky and requires proper understanding of the color change of the solution at the end of the chemical bath deposition (CBD) procedures. I would also suggest the solutions made for the CBD must be quite accurate in their concentrations and can be achieved by weighing near accurate quantities of respective salts on the chemical balance.

It is preferable to get done with the CdS layer by CBD on the very same day as absorber layer was deposited, as variations in the compositions of the absorber layers were observed when this was not done. It is better to have the sample inside the chamber under vacuum after the absorber layer deposition was finished and taken out just before the CBD was ready to go.

The 2SSS process device results are promising and it is believed devices with better uniformity and hence better throughput can be achieved with further study of a few complex mechanisms involved. With devices made with 2SSS process made at the CGS step it is necessary to carry on with this to the CIGS step to make even better comparison with the co-deposition results.

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